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SRI VASAVI ENGINEERING COLLEGE (AUTONOMOUS)

(Sponsored by Sri Vasavi Educational Society)
(Approved by **AICTE**, New Delhi & Recognized by **UGC** under section **2(f) & 12(B)**)
(Permanently affiliated to JNTUK, Kakinada, Accredited by **NBA** and **NAAC** with '**A**' Grade)
Pedatadepalli, **TADEPALLIGUDEM – 534 101.**W.G.Dist**. (A.P)**

Department of Electronics and Communication Engineering

Date: 04.09.2021

Minutes of the 5th meeting of BOS
(Held on 03.09.2021)

The ECE Department 5th meeting of Board of Studies (BOS) was conducted through online mode on 03.9.2021 at 11.00 A.M using ZOOM Application with following given link address.

https://us02web.zoom.us/j/83132873142.

Following external members have attended the meeting along with internal faculty members. The ECE HOD, Dr E. Kusuma Kumari, BOS Chairman headed the meeting.

Details of members attended:

S.No	Name of the BOS Member	Nominee	Address
1.	Dr.E. KusumaKumari	Chair person	Professor & Head, ECE, SVEC
2.	Prof.I. SanthiPrabha	University Nominee	Prof. in ECE Dept., University College of Engg., JNTUK, Kakinada
3.	Prof. NVSN. Sarma	Subject Expert	Director, IIIT Trichy Tiruchirapalli, Tamilnadu.
4.	Prof. M. VenugopalaRao	Subject Expert	Prof., ECE Dept., K.L.University, Vijayawada.
5.	Sri. Sunkavalli Siva Kumar	Alumni Nominee	Sr.Engineer,Qualcomm, Bangalore.
6.	All Faculty Members in Dept.	Members	ECE Dept., SVEC

The following are the key points discussed in the meeting.

- **Item No.1 : Chairperson, BOS has welcomed all the members and given the Opening Remarks.**

- **Item No.2: Review & Approval of the VII& VIII Sem of B. Tech ECE of V18 Reg.**

BOS members Reviewed the Course Structure and given Following Suggestions

- Change the Course title of Radar Systems to Radar Engineering (V18ECT20) in VII semester
- Change the Professional Elective course title from IoT: Concepts & Applications to IoT: Use cases (V18ECT24) in VII semester.
- Removal of topic of "Efficiency of Non Matched Filter in the syllabus of Radar Engg. Course (V18ECT20) in VII Semester.
- Rearrange the syllabus for course titled Optical Communication (V18ECT21) in VII semester.
- Add One more Text book for the Bio-Medical Instrumentation Course (V18ECT35) in VIII semester.

The approved course structure & Syllabus for the VII & VIII semesters of B. Tech ECE of V18 regulation was given in **Annexure-01**

- **Item No.3: Review & Approval the List of Open Elective Courses offered by ECE Dept., in VII & VIII Semesters B. Tech ECE of V18 Reg.**

BOS Members suggested that to Change the Open elective course title in VII Semester "Principles of Wireless, Cellular Mobile Comm. is to " Principles of Wireless Communication" (V18ECTOE4) and approved the Syllabus.

Approved List of Courses and Syllabus was given in **Annexure -02**

- **Item No. 4: Review & Approval of the Proposed Course Structure and Syllabi for the III and IV Semester of B. Tech ECE under V20 Regulation.**

- BOS members reviewed and suggested that try to include Machine Learning Topics in Course titled as Skill Oriented Course (V20ECSOC01) in the III and IV Semester of B. Tech ECE under V20 Regulation and approved the Syllabus.
- In the III semester, the Course titled Probability Theory & Stochastic Processes can be approved in the Basic Science BOS meeting. ECE BOS members were accepted to that proposal.
- Approved the Proposed Course Structure and Syllabi for the III and IV Semester of B. Tech ECE under V20 Regulation.

Approved List of Courses and Syllabus was given in **Annexure-03**

- **Item No. 5: Approval of List of Courses offered to EEE Department in III Semester of B. Tech EEE under V20 Regulation.**

  BOS members approved the Syllabus and details are given in **Annexure-04**

- **Item No. 6: Approval of Proposed course structure & syllabi for the courses offered in III & IV semesters of B. Tech ECT under V20 Regulation.**

  BOS members approved the Syllabus and details are given in **Annexure -05**.

- **Item No. 7: Approval of Proposed course structure and Syllabi for M. Tech Programme with specialization of Embedded Systems & VLSI under V21 Regulations.**

  BOS Members Suggested that to include the MOOCS courses in III semester of the M. Tech Programme, approved the Course Structure and Syllabus. The details are given in **Annexure -06**.

Finally, the chairperson thanked all the BOS members and faculty. The meeting was ended at 12.30 P.M

Dr. E. Kusuma Kumari,
Chairperson, BOS

Approved Course Structure & Syllabus for VII& VIII Semesters

COURSE STRUCTURE

(For V18 Regulation)

VII Semester

Sl. No.	Course Code	Category	Course Title	Hours per week			Credits
				L	T	P	C
1	V18ECT20	Professional Core Courses	Radar Engineering	3	0	0	3
2	V18ECT21	Professional Core Courses	Optical Communication	3	0	0	3
3	V18ECT22	Professional Core Courses	Digital Image Processing	3	0	0	3
4	V18ECT24 V18ECT25 V18ECT26	Prof. Elective Course	**Prof. Elective 3:** • IOT: Use Cases • CMOS Analog IC Design • Digital TV Engg.	3	0	0	3
5	V18ECT27 V18ECT28 V18ECT29	Prof. Elective Course	**Prof. Elective 4:** • Low Power IC Design • System On Chip • System Design Through Verilog	3	0	0	3
6	V18ECTOE4 V18ECTOE5 V18ECTOE6	Open Elective Course	**Open Elective-2:** • Principles of Wireless Comm. • Medical Electronics • Concepts of Embedded Systems	3	0	0	3
7	V18ECL11	Professional Core Course Lab	Microwave & Optical Comm. Lab	0	0	2	1
8	V18ECPR01	Project	Project	0	0	6	3
			Total	**18**	**0**	**8**	**22**

VIII Semester

Sl. No.	Course Code	Category	Course Title	Hours per week			Credits
				L	T	P	C
1	V18ECT30	Professional Core Course	Cellular Mobile Communication	3	0	0	3
2	V18ECT31 V18ECT32 V18ECT33	Professional Elective Course	**Prof. Elective 5:** • Electronics Measurements & Instrumentation • FPGA Architecture • Principles of Modern Wireless Communication Systems	3	0	0	3
3	V18ECT34 V18ECT35 V18ECT36	Professional Elective Course	**Prof. Elective 6:** • Satellite Communication • Biomedical Instrumentation. • Wireless Sensor Networks	3	0	0	3
4	V18ECTOE7 V18ECTOE8 V18ECTOE9	Open Elective Course	**Open Elective-3:** • Fundamentals of Digital Image & Video Processing • Embedded RTOS • Principles of Digital TV Engg.	3	0	0	3
5	V18ECPR02	Project	Project Contd.	0	0	16	8
			TOTAL	**12**	**0**	**16**	**20**

VII-Semester Syllabus

VII Sem.	Radar Engineering	Course Code:V18ECT20	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Derive the radar range equation and to solve some analytical problems. **[K2]**
- CO2: Describe the operation of CW and FMCW Radar systems. **[K2]**
- CO3: Illustrate the principle of each and every block of MTI and Pulse Doppler Radar **[K2]**
- CO4: Distinguish the different methods used for tracking targets. **[K2]**
- CO5: Relate the Noise Figure and Noise Temperature in Radar Receivers **[K2]**
- CO6: Explain the various components of radar receiver and its performance. **[K2]**

UNIT–I:

Basics of Radar: Introduction, Maximum Unambiguous Range, simple Radar range Equation, Radar Block Diagram and Operation, Radar Frequencies and Applications.

Radar Equation : Prediction of Range Performance, Minimum Detectable Signal, Receiver Noise, Modified Radar Range Equation, SNR, Probability of Detection, Probability of False Alarm, Integration of Radar Pulses, Radar Cross Section of Targets (simple targets-sphere, cone-sphere), Transmitter Power, PRF and Range Ambiguities, System Losses.

UNIT–II:

CW and Frequency Modulated Radar: Doppler Effect, CW Radar – Block Diagram, Isolation between Transmitter and Receiver, Non-zero IF Receiver, Receiver Bandwidth Requirements, Applications of CW radar.

FM-CW Radar: Range and Doppler Measurement, Block Diagram and Characteristics, FM-CW altimeter, Multiple Frequency CW Radar.

UNIT-III:

MTI and Pulse Doppler Radar: Introduction, Principle, MTI Radar with - Power Amplifier Transmitter and Power Oscillator Transmitter, Delay Line Cancellers – Filter Characteristics, Blind Speeds, Double Cancellation, Nth Cancellation Staggered PRFs. Range Gated Doppler Filters. MTI Radar Parameters, Limitations to MTI Performance, MTI versus Pulse Doppler Radar.

UNIT –IV:

Tracking Radar: Tracking with Radar, Sequential Lobing, Conical Scan, Mono pulse Tracking Radar – Amplitude Comparison Mono pulse (one- and two- coordinates), Phase Comparison Mono pulse, Tracking in Range, Acquisition and Scanning Patterns, Comparison of Trackers.

UNIT –V:

Detection of Radar Signals in Noise: Introduction, Matched Filter Receiver – Response Characteristics and Derivation, Correlation Detection and Cross-correlation Receiver, Matched Filter with Non-white Noise, Noise Figure and Noise Temperature.

UNIT –VI:

Radar Receivers –Displays – types. Duplexers – Branch type and Balanced type, Circulators as Duplexers.

Introduction to Phased Array Antennas – Basic Concepts, Radiation Pattern, Beam Steering and Beam Width changes, Series versus parallel feeds, Applications, Advantages and Limitations.

TEXT BOOKS:

1. Introduction to Radar Systems – Merrill I. Skolnik, TMH Special Indian Edition, 2nd Ed., 2007.
2. Radar Principles – Peebles, Jr., P.Z., Wiley, New York, 1998.
3. Microwave & Radar Engineering – G. SasibhushanaRao, Pearson Publications

REFERENCE BOOKS:

1. Introduction to Radar Systems, 3rd edition – M.I. Skolnik, TMH Ed., 2005
2. Microwave & Radar Engineering – M. Kulkarni, Umesh Publications, 3rd edition
3. Radar Engineering – GSN Raju, IK International.

VII Sem.	Optical Communication	Course Code:V18ECT21	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

CO1: Describe the overview of optical fiber communication, ray theory transmission and Concepts of modes.**[K2]**
CO2: Explain thoroughly the operation of optical sources, Quantum efficiency and power. **[K2]**
CO3: Classify different types of optical detectors and also explain the operation of optical Receiver.**[K2**
CO4: Illustrate the concept of power launching and power coupling for optical fibers. Discuss splicing techniques and connector losses. **[K3]**
CO5: Explain the types of fiber materials with their properties and fiber losses. **[K2]**
CO6:Construct optical link and becomes familiar with WDM concepts and measurement Techniques.**[K3]**

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UNIT I

Introduction - Historical development, the general system, advantages of optical fiber communications. Optical fiber wave guides - Ray theory transmission, Total Internal Reflection, Acceptance angle, Numerical Aperture, Skew rays, Cylindrical fibers- Modes, V-number, Mode coupling, Step Index fibers, Graded Index fibers, Single mode fibers - Cut off wavelength, Mode Field Diameter, Effective Refractive Index, Related problems.

UNIT II

Optical sources-LEDs, Structures, Materials, Quantum efficiency, Power, Modulation, Power bandwidth product. Injection Laser Diodes- Modes, Threshold conditions, Laser diode rate equations, External quantum efficiency, resonant frequencies, Reliability Considerations.

UNIT III

Optical detectors- Physical principles of PIN and APD, Detector response time, Temperature effect on Avalanche gain, Comparison of Photo detectors, Optical receiver operation - Fundamental receiver operation, Digital signal transmission, error sources, Receiver configuration, Digital receiver performance, Probability of Error, Quantum limit, Analog receivers. Related problems.

UNIT IV

Fiber materials - Glass, Halide, Active glass, Chalgenide glass, Plastic optical fibers. Signal Degradation in optical fibers - Attenuation, Absorption, Scattering and Bending losses, Core and Cladding losses, Information capacity determination, Group delay, Types of Dispersion: Material dispersion, Wave-guide dispersion, Polarization-Mode dispersion, Intermodal dispersion, Pulse broadening in Graded index fiber, Related problems.

UNIT V

Source to fiber power launching-Output patterns, Power coupling, Power launching, Equilibrium Numerical Aperture, Lensing Schemes for Coupling, Laser diode to fiber coupling. Fiber to Fiber joints – Mechanical misalignment, Fiber related losses, End face preparation, Fiber Splicing-Splicing techniques, Splicing single mode fibers, Optical fiber Connectors-

Connector types, Single mode fiber connectors, Connector return loss, Multimode fiber joints, Single mode fiber joints.

UNIT VI

Optical system design - Point-to- point links- System considerations, Link power budget, Rise time budget with examples, Line coding in Optical links, Operational Principles of WDM, Measurement of Attenuation and Dispersion, Eye pattern.

TEXT BOOKS:

1. Optical Fiber Communications – Gerd Keiser, McGraw-Hill International edition, 3rd Edition, 2000.
2. Fiber Optic Communication Systems – Govind P. Agarwal, John Wiley, 3rd Edition, 2004.

RERFERENCES:

1. Fiber Optic Communications – D.K. Mynbaev, S.C. Gupta and Lowell L. Scheiner, Pearson Education,2005.
2. Text Book on Optical Fiber Communication and its Applications – S.C.Gupta, PHI, 2005.
3. Fiber Optic Communications – Joseph C. Palais, 4th Edition, Pearson Education, 2004.

VII Sem.	Digital Image Processing	Course Code:V18ECT22	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

CO1. Illustrate the different Transforms Techniques & their use in Image Processing Applications**(K3)**
CO2. Examine Spatial & frequency domain filtering like smoothing & sharpening Operation son Images **(K4)**
CO3. Analyze Restoration operations/techniques on Images**(K4)**
CO4. Describe the Image compression Techniques and multi-resolution processing on Images**(K3)**
CO5. Analyze morphological operations on Images & Image segmentation**(K4)**
CO6. Illustrate the different color Image Processing Techniques on Images**(K3)**

UNIT-I

Introduction: Introduction to Image Processing, Fundamental steps in digital image processing, components of an image processing system, image sensing and acquisition, image sampling and quantization, some basic relationships between pixels, an introduction to the mathematical tools used in digital image processing.

Image Transforms: Need for image transforms, Discrete Fourier transform (DFT) of one variable, Extension to functions of two variables, some properties of the 2-D Discrete Fourier transform, Walsh Transform. Hadamard transform, Haar Transform, Slant transform, Discrete Cosine transform, Discrete Sine Transform, Comparison of different image transforms.

UNIT-II

Intensity Transformations and Spatial Filtering: Some basic intensity transformation functions, histogram processing, fundamentals of spatial filtering, smoothing spatial filters, and sharpening spatial filters.

Filtering in the Frequency Domain: The Basics of filtering in the frequency domain, image Smoothing using frequency domain filters, Image Sharpening using frequency domain filters, Selective filtering.

UNIT-III

Image Restoration and Reconstruction: A model of the image degradation / Restoration process, Noise models, restoration in the presence of noise only-Spatial Filtering, Periodic Noise Reduction by frequency domain filtering, Linear, Position –Invariant Degradations, Estimating the degradation function, Inverse filtering, Minimum mean square error (Wiener) filtering, geometric mean filter .

UNIT-IV

Image compression: Fundamentals, Basic compression methods: Huffman coding, Arithmeticcoding,LZWcoding,Run-Lengthcoding,Symbol-Basedcoding,Bit-Planecoding,BlockTransformcoding,

Wavelets and Multi resolution Processing: Image pyramids, sub band coding, Multi resolution expansions, wavelet transforms in one dimensions &two dimensions, Wavelet coding.

UNIT-V

Image segmentation: Fundamentals, point, line, edge detection, thresholding and region – based segmentation.

Morphological Image Processing: Erosion and dilation, opening and closing,basic morphological algorithms for boundary extraction, thinning, gray scale morphology.

UNIT-VI

Color image processing: color fundamentals, color models, pseudo color image processing, basics of full color image processing, color transformations, smoothing and sharpening. Image segmentation based on color, noise in color images, color image compression.

TextBooks:

1. R.C. Gonzalez and R.E.Woods,Digital ImageProcessing,3rdedition,PrenticeHall,2008.
2. Jayaraman,S.Esakkirajan,andT.Veerakumar,"DigitalImageProcessing",TataMcGraw-Hill Education,2011.

Reference Books:

1. AnilK.Jain,"FundamentalsofDigitalImageProcessing",PrenticeHallofIndia,9thEdition,IndianReprint,2002.
2. B.Chanda, D.Dutta Majumder, "Digital ImageProcessingandAnalysis",PHI,2009.

VII Sem.	IOT: Use Cases (Professional Elective-III)	Course Code:V18ECT24	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Describe M2M and IOT Technologies. **[K2]**
- CO2: Explain the layers and protocols in IOT. **[K2]**
- CO3: Describe various communication technologies used in IOT. **[K2]**
- CO4: Illustrate various hardware components required for IOT applications. **[K2]**
- CO5: Discuss the cloud technologies and their services. **[K2]**
- CO6: Explain the IoT Applications. **[K2]**

UNIT I – INTRODUCTION [1]

Introduction from M2M to IoT - An Architectural Overview, building architecture, Main design principles and needed capabilities, An IoT architecture outline, M2M and IoT Technology Fundamentals - Devices and gateways.

UNIT II – IOT PROTOCOLS [2]

Functionality of Layers in IoT –Study of protocols - Wireless HART, Z-Wave, 6LoWPAN, RPL, CoAP, MQTT.

UNIT III - COMMUNICATION TECHNOLOGIES IN IOT [2, 4]

Study of IoT Connectivity –IEEE 802.15.4,Zigbee, LPWAN, Wi-Fi, Bluetooth, 5G Era.

UNIT IV - SYSTEM HARDWARE [3, 4]

Sensors, Actuators, Radio Frequency Identification, Introduction to Embedded Devices for IoT - RASPBERRY PI, BeagleBone black.

UNIT V – Cloud Computing [3, 4]

Data Collection, Storage and Computing Using a Cloud Platform for IoT Applications/Services, AWS for IoT-Introduction to Amazon EC2.

UNIT VI - IOT APPLICATIONS [2, 3]

Applications - Smart and Connected Cities, Public Safety, Agriculture, and Healthcare.

TEXTBOOKS:

1. "From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence", Jan Holler, Vlasios Tsiatsis, Catherine Mulligan, Stefan Avesand, StamatisKarnouskos, David Boyle, 1st Edition, Academic Press, 2014.
2. IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry, and Cisco Press 800 East 96th Street Indianapolis, Indiana 46240 USA.
3. "Internet of Things (A Hands-on- Approach)", Vijay Madisetti and ArshdeepBahga, 1stEdition, VPT, 2014.
4. Internet of Things - By Raj Kamal, McGraw-Hill Education. Copyright.

REFERENCE BOOKS:

1. From Internet of Things to Smart Cities: Enabling Technologies - edited by Hongjian Sun, Chao Wang, Bashar I. Ahmad, CRC Press -2018.
2. Bernd Scholz-Reiter, Florian Michahelles, “Architecting the Internet of Things”, ISBN 978-3-642-19156-5 e-ISBN 978-3-642-19157-2, Springer.
3. IOT (Internet of Things) Programming: A Simple and Fast Way of Learning IOT, David Etter.

VII Sem.	CMOS ANALOG IC DESIGN (Professional Elective-III)	Course Code:V18ECT25	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Describe the Large and Small signal models of different Analog Devices**(K2)**
- CO2: Analyse the various types of current mirrors**.(K3)**
- CO3: Analyse the different types of single stage MOS amplifiers**.(K3)**
- CO4: Describe the Noise modelling of Various Circuit Elements**.(K2**)
- CO5: Illustrate the construction and working of OP-AMP**.(K3)**
- CO6: Illustrate the types of CMOS Comparators **.(K3)**

UNIT -I: Integrated circuit Devices and Modelling

Semiconductors and p-n junction: diodes reverse biased diodes, graded junctions, large signal junction capacitance and forward biased junctions small signal model of forward biased diode

The MOS Transistor**:** symbol for MOS Transistors, basic Operation, and Large signal modelling small signal modelling.

Bi-Polar Transistors: basic Operation, Large signal modelling small signal modelling

UNIT -II: Basic Current Mirrors

Basic CMOS current Mirrors, source Degenerated current mirror, Cascade current Mirror and Wilson Current Mirror, bipolar current mirror and Current mirror with Beta Helper.

UNIT -III: Single Stage Amplifiers

Common source amplifier, Source follower, common gate Amplifier, Cascode Gain stage amplifier and MOS Differential Amplifiers. Frequency response of Amplifiers.

UNIT -IV: Noise Analysis and Modelling

Time Domain Analysis of Noise**:** RMS, SNR, Units of dBm& Noise summation**.**

Frequency Domain Analysis of Noise**:** Noise spectral Density, White Noise, Flicker Noise, Noise filtering & Noise bandwidth**.**

Noise models for circuit elements**:** Resistors, Diodes, Transistors and MOSFETS

UNIT -V: CMOS Operational Amplifiers & Compensation

Block diagram of Op-amp, op-amp gain, frequency response &Slew Rate, op-amp Compensation

UNIT -IV: Comparators

Characterization of Comparator, Two-Stage,Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete- Time Comparators.

TEXT BOOKS:

1. Analog Integrated Circuit Design- David A.Johns, Ken Martin, Wiley Student Edn,2013.

2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press, International Second Edition/Indian Edition,2010.

REFERENCES:

1. Analysis and Design of Analog Integrated Circuits- Paul R. Gray, Paul J. Hurst, S. Lewis and R. G. Meyer, Wiley India, Fifth Edition,2010.

2. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, Second Edition

VII Sem.	Digital TV Engineering (Professional Elective-III)	Course Code:V18ECT26	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Illustrate the fundamentals of television engineering. **[K2]**
- CO2:Explain the colour TV transmission and reception **[K2]**
- CO3: Compare Digital TV transmission standards **[K4]**
- CO4: Discuss factors affecting system noise and transmission errors **[K2]**
- CO5: Explain the Digital TV transmission and reception. **[K2]**
- CO6: Describe the operation of LCD and Plasma screens **[K2]**

UNIT I

Introduction: TV transmitter and receivers, synchronization

Television Pictures: Geometric form and aspect ratio, image continuity, interlaced scanning, picture resolution

Composite video signal: Horizontal and vertical sync details

TV Signal Transmission: VSB transmission, standard channel BW, TV transmitter

UNIT II

Colour Television: Perception of brightness and colours, additive colour mixing, video signals for colours, luminance signal, colour difference signals, encoding of colour difference signals, formation of chrominance signals, PAL encoder, PAL colour receiver

UNIT III

Digital Television Transmission Standards: ATSC terrestrial transmission standard, vestigial sideband modulation, DVB -T transmission standard, ISDB-T transmission standard, channel allocations, antenna height and power, MPEG-2.

UNIT IV

Performance Objectives for Digital Television: System noise, external noise sources, transmission errors, error vector magnitude, eye pattern, interference, co-channel interference, adjacent channel interference, analog to digital TV, transmitter requirements.

UNIT V

Digital Television: Digital System Hardware, Signal Quantization and Encoding, Digital Satellite Television, Direct to Home Satellite Television, Digital TV Receiver, Merits of Digital TV Receivers

UNIT VI

LCD and Plasma Screens: LCD Technology, LCD Matrix types and operation, LCD Screens for Television, Plasma and conduction of charge, Plasma TV Screens, Plasma Color Receiver, LCD color receiver

Text Books:

1. Modern Television Practice: Transmission, Reception and Applications- R. R.Gulati, 4th Revised edition, New Age International Publishers.
2. Television and Video Engineering – A.M. Dhake, 2nd Edition, Tata McGraw Hill Publishers.
3. Fundamentals of Digital Television Transmission- Gerald W. Collins, John Wiley & Sons.
4. Television engineering and video systems – R G Gupta, Tata McGraw Hill Publishers.

References

1. Basic Television and Video Systems – Bernard Grob, McGrawHill Publishers.
2. Monochrome and Colour Television - R RGulati, New Age International Publishers.
3. Colour Television, Theory and Practice - S.P.Bali, Tata McGraw-Hill Publishers.

VII Sem.	Low Power IC Design (Professional Elective-IV)	Course Code:V18ECT27	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Explain the need of Low power circuit design **(K2)**.
- CO2: Describe the different architectural approaches **(K2)**.
- CO3: Analyze Low-Power Design Approaches**(K4).**
- CO4: Analyze and design Low-Voltage Low-Power Adders circuits**(K4).**
- CO5: Analyze and design Low-Voltage Low-Power Multiplier circuits**(K4).**
- CO6: Analyze and design of Low-Voltage Low-Power Memories**(K4).**

UNIT–I:

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation–Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects.

UNIT–II:

Supply Voltage Scaling for Low Power: Device Feature Size Scaling, Constant-Field Scaling, Constant-Voltage Scaling, Architectural-Level Approaches: Parallelism for Low Power, Pipelining for Low Power, Combining Parallelism with Pipelining.
Voltage Scaling Using High-Level Transformations: Multilevel Voltage Scaling Challenges in MVS Voltage Scaling Inter faces, Static Timing Analysis Dynamic Voltage and Frequency Scaling.

UNIT-III

Low-PowerDesignApproaches: Low-PowerDesignthroughVoltageScaling–VTCMOScircuits,MTCMOScircuits,ArchitecturalLevelApproach–PipeliningandParallelProcessing Approaches. Power Gating, Clock Gating Versus Power Gating, Power-Gating Issues.

UNIT–IV:

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques –Trends of Technology and Power Supply Voltage.

UNIT-V

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types ofMultiplierArchitectures,BraunMultiplier,Baugh-WooleyMultiplier,IntroductiontoWallace Tree Multiplier.

UNIT–VI:

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Pre-charge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

TEXTBOOKS:

1. CMOS Digital Integrated Circuits–Analysis and Design–Sung-Mo Kang, Yusuf Leblebici, TMH,2011.
2. Low-Voltage, Low-Power VLSI Subsystems–Kiat-SengYeo,KaushikRoy,TMH ProfessionalEngineering,1st edition,2004

REFERENCEBOOKS:

1. IntroductiontoVLSISystems:ALogic,CircuitandSystemPerspective–Ming-BO Lin, CRCPress,2011
2. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad,JohnWiley& Sons,2000.
3. Practical Low Power Digital VLSI Design–Gary K.Yeap,Kluwer AcademicPress,2002.
4. Leakage in Nanometer CMOS Technologies–SivaG.Narendran,Anatha Chandrakasan, Springer,2005.

VII Sem.	System on Chip (Professional Elective-IV)	Course Code:V18ECT28	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Describe SOC System Approach, design and its Architecture.**[K2]**
- CO2: Discuss the selection of processor and its micro architecture for SOC**[K2]**
- CO3: Describe Memory Design for SOC **[K2]**
- CO4: Explain the concepts of bus models and Interconnect Architectures **[K2]**
- CO5: Describe the overview of Zynq SOC**[K2]**
- CO6: Explain the SOC based Applications. **[K2]**

UNIT – I: Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, an approach for SOC Design, System Architecture and Complexity.

UNIT – II : Processors: Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT – III : Memory Design for SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT – IV : Interconnect Customization and Configuration: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance Specific design, Customizable Soft Processor.

UNIT-V: Zynq system on chip design overview: interfacing and signals, interconnects, Memory and interrupts.

UNIT – VI: Application Studies / Case Studies: SOC Design approach, Design and evaluation - AES algorithms, Image compression – JPEG compression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC-Louise H. Crockett Ross A. Elliot Martin A. Enderwitz Robert W. Stewart
3. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer

REFERENCE BOOKS:

1. Co-Verification of Hardware and Software for ARM System on Chip Design

(Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.

2. System on Chip Verification – Methodologies and Techniques – Prakash Rashinkar,

Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

VII Sem.	System Design Through VERILOG (Professional Elective-IV)	Course Code:V18ECT29	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Outline basic concepts of RTL code for digital circuits **K2**
- CO2: Model RTL codes for digital circuit at gate level **K3**
- CO3: Model RTL codes for digital circuit at behavioural level **K3**
- CO4: Model RTL codes for digital circuit at data flow and switch level **K3**
- CO5: Ouline the concepts of task, function and complier directives **K2**
- CO6: Analyze Synthesize of Combinational and Sequential Circuits **K4**

UNIT-I
INTRODUCTIONTOVERILOG:

Verilog as HDL, Levels of design description, concurrency, module, simulation and synthesis, test bench, functional verification, programming language interface (PLI), simulation and synthesis tools.

LANGUAGECONSTRUCTSANDCONVENTIONS:
Introduction, keywords, identifiers, whitespace characters, comments, numbers, strings, logic values, data types, scalars and vectors, parameters, memory, operators, system tasks.

UNIT-II
GATELEVELMODELLING:

Introduction, and gate primitive, module structure, other gate primitives, illustrative examples, tristate gates, array of instances of primitives, design of Flip flops with gate primitives, delays, strengths and contention resolution, net types, design of basic circuits.

UNIT-III
BEHAVIORALMODELLING:

Introduction, operations and assignments, initial construct, always construct, examples, assignments with delays, wait construct, multiple always blocks, designs at behavioral level, blocking and non-blocking assignments, the case statement, if and if else constructs, assign-De assign construct, repeat construct, FOR loop, the disable construct, While loop, Forever loop, parallel blocks, force-release construct, event.

UNIT-IV
DATA FLOWLEVEL MODELLING

Introduction, continuous assignment structures, delays and continuous assignments, assignment to vectors.

SWITCH LEVEL MODELLING

Basic transistor switches, CMOS switch, Bidirectional gates and time delays with switch primitives, instantiations with strengths and delays, strength contention with triregnets, switch level modeling for NAND, NOR and XOR.

UNIT-V

SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES: Introduction, System Tasks and Functions, File based Tasks and Functions, Compiler Directives, Hierarchical Directives, User-defined Primitives (UDP), FSM Design (Moore and Melay Machines).

UNIT-VI

SYNTHESISOFCOMBINATIONAL ANDSEQUENTIAL LOGIC USINGVERILOG: Synthesis of Combinational logic: Net list of structured primitives, a set of continuous assignment statements and level sensitive cyclic behavior with examples, Synthesis of priority structures, exploiting logic don't care conditions.

Synthesis of sequential logic with latches: Accidental synthesis of latches and Intentional synthesis of latches, Synthesis ofsequentiallogicwithflip-flops,Synthesisofexplicitstatemachines.

TEXTBOOKS:

1. Design through VerilogHDL —T.R.PadmanabhanandB. BalaTripuraSundari, WSE,IEEEPress,2004.
2. Advanced Digital Design withVerilog HDL—MichaelD.Ciletti,PHI,2005.

REFERENCES:

1. FundamentalsofLogicDesignwithVerilog—Stephen.BrownandZvonkoVranesic,TMH,2005.
2. AVerilogPrimier—J.Bhasker,BSP,2003.

VII Sem.	Microwave & Optical Comm. Lab	Course Code:V18ECL11	L	T	P	C
			0	0	3	1

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

CO1. Sketch the characteristics of various Microwave & Optical sources **(K3)**

CO2. Compute the various Parameters of Microwave & Optical Components **(K3)**

CO3. Measure the radiation pattern of Horn antenna and reflector antenna. **(K5)**

CO4. Analyze a rectangular microstrip patch antenna using HFSS software **(K4)**

Minimum Twelve Experiments to be conducted:

Part – A (Any 7 Experiments):

1. Reflex Klystron Characteristics.
2. Gunn-Diode Characteristics.
3. Attenuation Measurement.
4. Directional Coupler Characteristics.
5. Impedance and Frequency Measurement.
6. Scattering parameters of Circulator.
7. Scattering parameters of Magic Tee.
8. Radiation Pattern of Horn and Parabolic Antennas.
9. Synthesis of Microstrip antennas (Rectangular Structure) Using HFSS.

Part – B (Any 5 Experiments):

10. Characterization of LED.
11. Characterization of Laser Diode.
12. Intensity modulation of Laser output through an optical fiber.
13. Measurement of Data rate for Digital Optical link.
14. Measurement of NA.
15. Measurement of losses for Analog Optical link.

Equipment required for Laboratories:

1. Klystron Power Supply, Klystron mount
2. VSWR Meter
3. Micro Ammeter
4. Multi meter
5. CRO
6. GUNN Power Supply, Pin Modulator
7. Crystal Diode detector
8. Attenuator
9. Frequency Meter
10. Slotted line carriage
11. Probe detector

12. Wave guide shorts
13. SS Tuner
14. Directional Coupler
15. E, H, Magic Tees
16. Circulators, Isolator
17. Matched Loads
18. Pyramidal Horn and Parabolic Antennas
19. Turntable for Antenna Measurements
20. HFSS Software
21. Fiber Optic Analog Trainer based LED
22. Fiber Optic Analog Trainer based laser
23. Fiber Optic Digital Trainer
24. Fiber cables - (Plastic, Glass)

VIII-Semester Syllabus

VIII Sem.	Cellular & Mobile Communication	Course Code:V18ECT30	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

CO1: Demonstrate the limitations of conventional mobile telephone systems; Understand the concepts of cellular systems. **[K2]**
CO2: Illustrate the concept of frequency Reuse channels, deduce Co- channel Interference reduction factor **[K2]**
CO3: Understand the frequency management, channel assignment strategies and Antennas in cellular systems.**[K2]**
CO4:Discuss the concepts of Handoff, dropped calls and cell splitting, Intersystem Handoff. **[K2]**
CO5: Explain the knowledge about GSM architecture and GSM channels, multiple Access schemes like FDMA,TDMA and CDMA. **[K2]**
CO6: Summarize the concepts of upcoming technologies like 3G, 4G etc. **[K2]**

UNIT-I CELLULAR MOBILE RADIO SYSTEMS: Introduction to Cellular Mobile System, uniqueness of mobile radio environment, operation of cellular systems, consideration of the components of Cellular system, Hexagonal shaped cells, Analog and Digital Cellular systems.

CELLULAR CONCEPTS: Evolution of Cellular systems, Concept of frequency reuse, frequency reuse ratio, Number of channels in a cellular system, Cellular traffic: trunking and blocking, Grade of Service; Cellular structures: macro, micro, pico and femto cells; Cell splitting, Cell sectoring.

UNIT-II INTERFERENCE: Types of interferences, Introduction to Co-Channel Interference, real time Co-Channel interference, Co-Channel measurement, Co-channel Interference Reduction Factor, desired C/I from a normal case in a Omni directional Antenna system, design of Antenna system, antenna parameters and their effects, diversity receiver, non-cochannel interference-different types.

UNIT-III FREQUENCY MANAGEMENT AND CHANNEL ASSIGNMENT: Numbering and grouping, setup access and paging channels, channel assignments to cell sites and mobile units: fixed channel and non-fixed channel assignment, channel sharing and borrowing, overlaid cells. CELL COVERAGE FOR SIGNAL AND TRAFFIC: Signal reflections in flat and hilly terrain, effect of human made structures, phase difference between direct and reflected paths, straight line path loss slope, and general formula for mobile propagation over water and flat open area, near and long distance propagation, antenna height gain, form of a point to point model.

UNIT-IV HANDOFF STRATEGIES Concept of Handoff, types of handoff, handoff initiation, delaying handoff, forced handoff, mobile assigned handoff, intersystem handoff, vehicle locating methods, dropped call rates and their evaluation.

UNIT-V DIGITAL CELLULAR NETWORKS: GSM architecture, GSM channels, multiple access schemes; FDMA, TDMA, CDMA, OFDMA;

UNIT-VI HIGHER GENERATION CELLULAR STANDARDS: 3G System architecture (UMTS) enhancements in 4G standard, Architecture and representative protocols, introduction to 5G.

TEXTBOOKS:

1. Mobile Cellular Telecommunications – W.C.Y. Lee, Tata McGraw Hill, 2rd Edn, 2006.
2. Principles of Mobile Communications – Gordon L. Stuber, Springer International 2nd Edition, 2007.

REFERENCES:

1. Wireless Communications – Theodore. S. Rapport, Pearson education, 2nd Edn, 2002.
2. Wireless and Mobile Communications – Lee McGraw Hills, 3rd Edition, 2006. 3. Mobile Cellular Communication – G Sasibhushana Rao Pearson
3. Wireless Communication and Networking – Jon W. Mark and Weihua Zhqung, PHI, 2005.
4. Wireless Communication Technology – R. Blake, Thompson Asia Pvt. Ltd., 2004.

VIII Sem.	Electronics Measurements & Instrumentation (Professional Elective-V)	Course Code:V18ECT31	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

CO1. Select the instrument to be used based on the requirements**.[K2]**
CO2. Understand the design of oscilloscopes for different applications**.[K2]**
CO3. Explain different signal generators and analyzers**.[K2]**
CO4. Understand the design of different types of Bridge circuits for different Applications.**[K2]**
CO5. Explain and Design different types of transducers for different Applications. **[K2]**
CO6. Explain different types of transducers for measurement of Physical parameters. **[K2]**

UNIT-I

Performance characteristics of instruments, Static characteristics, Accuracy, Resolution, Precision, Expected value, Error, Sensitivity. Errors in Measurement, Dynamic Characteristics- speed of response, Fidelity, Lag and Dynamic error. DC Voltmeters- Multi-range, Range extension/Solid state and differential voltmeters, AC voltmeters- multirange, range extension, shunt. Thermocouple type RF ammeter, Ohmmeters series type, and shunt type, Multi-meter for Voltage, Current and resistance measurements.

UNIT-II

Oscilloscopes CRT features, vertical amplifiers, horizontal deflection system, sweep, trigger pulse, delay line, sync selector circuits, simple CRO, triggered sweep CRO, Dual beam CRO, Dual trace oscilloscope, sampling oscilloscope, storage oscilloscope, digital readout oscilloscope, digital storage oscilloscope, Lissajous method of frequency measurement, standard specifications of CRO, Probes for CRO-Active & Passive, attenuator types.

UNIT-III

Signal Generator- fixed and variable, AF oscillators, Standard and AF sine and square wave signal generators, Function Generators, Square pulse, Random noise, sweep, Arbitrary waveform. Wave Analyzers, Harmonic Distortion Analyzers, Spectrum Analyzers, Digital Fourier Analyzers.

UNIT-IV

DC Bridges: Measurement of Resistance-Wheatstone's Bridge, Kelvin's Bridge. AC Bridges: Measurement of inductance- Maxwell's bridge, Hay's bridge, Anderson Bridge. Measurement of capacitance-Schering's Bridge. Measurement of Frequency-Wien Bridge, Errors and precautions in using bridges.Q-meter.

UNIT-V

Transducers- active & passive transducers : Resistance, Capacitance, inductance; Strain gauges, LVDT, Piezo Electric transducers, Resistance Thermometers, Thermocouples, Thermistors, Sensistors.

UNIT-VI

Measurement of physical parameters- Force,Pressure, Velocity, Acceleration, Humidity, Moisture, Proximity, Displacement.Data acquisition systems.

TEXTBOOKS:

1. Electronic Instrumentation, second edition-H.S. Kalsi, Tata McGrawHill,2004.
2. Modern Electronic Instrumentation and Measurement Techniques–A.D. Helfrick and W.D.Cooper, PHI, 5thEdition, 2002.

REFERENCES:

1. Electronic Instrumentation &Measurements- David A. Bell, PHI, 2nd Edition,2003.
2. Electronic Test Instruments, Analog and Digital Measurements-Robert A. Witte, Pearson Education, 2nd Edition, 2004.
3. Electronic Measurements & Instrumentations by K. LalKishore, Pearson Education-2005.
4. Electronic Measurements & Instrumentation by UdayA.Bakshi& Ajay V. Bakshi Technical Publications

VIII Sem.	FPGA Architecture (Professional Elective-IV)	Course Code:V18ECT32	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

CO1: Describe Low end programmable devices.**[K2]**
CO2: Explain FPGA basics.**[K2]**
CO3: Comprehend Spartan 6 basics.**[K2]**
CO4: Use Virtex 5 clock sources and FIFO. Comprehend various I/O standards.**[K2]**
CO5: Use Memory, DSP blocks in complex designs. Comprehend SerDes.**[K2]**
CO6: Comprehend JTAG. Distinguish RISC based Soft processors from Xilinx, Aletra.**[K2]**

UNIT-I
DESIGNING WITH PROGRAMMABLE LOGIC DEVICES:
Read only Memories, Programmable logic Arrays (PLA), Programmable Array logic (PAL), Programmable logic Devices (PLD) Skew, setup, hold time.

UNIT-II
DESIGNING WITH FPGA:
Logic implementation options, Technology trends, Simple SRAM programmable FPGA architecture, Xilinx 3000 series FPGAs, Programmable interconnects, Xilinx 4000 series FPGAs, Programming the FPGA.

UNIT-III
SPARTAN 6 ARCHITECUTUTE:
Spartan 6 Device features- 6 input LUT, Slice, Single Port RAM, Dual Port RAM, ROM, Distributed RAM, 32 x 6, 64 x 1, 128 x 1, Distributed RAM timings, Shift Registers, Multiplexers, Interconnect, PLL, DCM, DSP Slice.

UNIT-IV
VIRTEX 5 ARCHITECTURE:
Clock resources-Global clocks, regional clocks, Clock buffer, Clock Gating.Clock Tree, Clock De-skew, True Dual port RAM. Write modes, FIFO architecture, empty flags, almost empty flags, almost fill flags, full flag, cascading FIFOS, connecting FIFOs in parallel, designing Large multiplexer 4xl, 8xl, 16xl. Control impedance, I/O primitives. I/O supported standards, LVDS.

UNIT-V
STARATIX V ARCHITECTURE:
ALM Block diagram, ALM operating modes, ALM in Arithmetic mode, Types of embedded memory, Control clocking, Memory features, Memory modes, DSP block features, operational modes, DSP block architecture in 27 X 27 mode, independent complex multiplier mode, I/O features mixing voltage referenced and non-voltage referenced standard I/O features standards. Dynamic OCT.LVDS SerDes block diagram and features, Differential Receiver Block diagram and features.

UNIT-VI

SOFT PROCESSORS:

JTAG, programming through JTAG, IEEE 1149.1 Boundary scan testing, programmable power technology, Features of Soft processors, Nios-II, Microblaze.

TEXT BOOKS:

1. Charles H Roth Jr “Digital System Design using VHDL”, second edition, 2008.
2. Spartan 6 family overview.
3. Virtex 5- User Guide.
4. Staratix V Device Hand Book.
5. Nios-II, Microblaze Features – Altera, Xilinx.

REFERENCES:

1. J. Old Field,R.Dorf, “Field Programmable Gate Arrays”, John Wiley & Sons, New York, 1995.
2. S. Trimberger, Edr.“Field Programmable Gate Arrays Technology”, Kluwer Academic Publications, 1994.
3. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books, 2002.

VIII Sem.	Principles of Modern Wireless Communication Systems (Professional Elective-V)	Course Code:V18ECT33	L	T	P	C
			3	0	0	3

Syllabus Details

CO1: Describe how to measure the performance of wireless system, in multipath Environment **[K2]**
CO2: Summarize about Wireless Channel. **[K2]**
CO3: Explain Principle and properties of CDMA. **[K2]**
CO4: Discuss the working and advantages of MIMO wireless communication systems **[K2]**
CO5: Explain the principle and advantages of OFDM system**[K2]**
CO6: Describe of various modern wireless communication technologies **[K2]**

UNIT-I

Principles of Wireless Communication: The wireless communication environment, modelling of wireless systems, system model for narrowband signals, Rayleigh fading wireless channel, BER performance of wireless systems, channel estimation in wireless systems, Diversity in wireless communication, multiple antenna receive model, BER in multiple antenna system, channel estimation in multiple antenna system.

UNIT-II

Wireless Channel: Basics of Wireless Channel Modelling, Maximum Delay Spread, RMS Delay Spread, RMS Delay Based on Average Power Profile, Average Delay Spread in Outdoor Cellular Channels, Coherence Bandwidth in Wireless Communications, Relation between ISI and Coherence Bandwidth.

UNIT-III

Code Division Multiple Access: Fundamentals of CDMA codes, Spreading codes based on Pseudo-Noise sequences, correlation properties of random CDMA spread sequences, Multi-user CDMA, Advantages of CDMA, CDMA near far problem and power control.

UNIT-IV

Multiple Input Multiple Output Wireless Communications: Introduction to MIMO wireless Communications, MIMO System model, MIMO zero forcing (ZF) receiver, MIMO MMSE receiver, Singular Value Decomposition (SVD) of the MIMO channel, MIMO capacity, Asymptotic MIMO capacity, MIMO beam forming.

UNIT-V

Orthogonal Frequency Division Multiplexing: Introduction to OFDM, multicarrier transmission, cyclic prefix in OFDM, BER for OFDM, MIMO-OFDM, effect of frequency offset in OFDM, Peak to Average Power ratio in OFDM, SC-FDMA.

UNIT-VI

Recent advancements in wireless technology: Introduction to 4G LTE, VoLTE, 5G Technology, NOMA and Massive MIMO.

Text Books:

1. Aditya K. Jagannatham, “Principle of Modern Wireless Communication Systems: Theory and practice” 1st Edition, McGrawHill Publication
2 Theodore S. Rappaport, “Wireless Communications: Principles and Practice” Second Edition, Pearson Education

Reference Books:

1. Simon Haykin, MichaleMoher, “Modern Wireless Communications”, Pearson.
2. Xiaodong Wang, H. Vincent Poor, “Wireless Communication Systems: Advanced Techniques for Signal Reception”, Pearson 5 Proakis J.J.,D Wozencraft J.M. and Jacobs I.M., Principles of Communication Engineering, John Wiley

VIII Sem.	Satellite Communication (Professional Elective-VI)	Course Code:V18ECT34	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

CO1. Describe the basic concepts of Satellite Communications & analyze the concepts of Orbital mechanics & Launchers **(K4)**

CO2.Discuss the major Sub-Systems of a Satellite **(K2)**

CO3.Design the Communication Link for Satellite **(K4)**

CO4.Compare the various Multiple Access Techniques **(K3)**

CO5.Analyze the various sub-systems used in Earth stations & review the different orbits **(K4)**

CO6.Analyze the Satellite Navigation & the Global positioning system **(K4)**

UNIT-I

Introduction: Origin of Satellite Communications, Historical Back-ground, Basic Concepts of Satellite Communications, Frequency allocations for Satellite Services, Applications, Future Trends of Satellite Communication.

Orbital Mechanics and Launchers: Orbital Mechanics, Look Angle determination, Orbital perturbations, Orbit determination, launches and launch vehicles, Orbital effects in communication systems performance.

UNIT-II

Satellite Subsystems: Attitude and orbit control system, telemetry, tracking, Command &monitoring, power systems, communication subsystems, Satellite antenna Equipment reliability and Space qualification.

UNIT-III

Satellite Link Design: Basic transmission theory, system noise temperature and G/T ratio, Design of down links, up link design, Design of satellite links for specified C/N, System design example.

UNIT-IV

Multiple Access: Frequency division multiple access (FDMA), Inter modulation, Calculation of C/N. Time division Multiple Access (TDMA), Frame structure, Examples. Satellite Switched TDMA Onboard processing, DAMA, Code Division Multiple access (CDMA), Spread spectrum transmission and reception.

UNIT-V

Earth Station Technology: Introduction, Transmitters, Receivers, Antennas, Tracking systems, Terrestrial interface, Primary power test methods.

Low Earth Orbit and Geo-Stationary Satellite Systems: Orbit consideration, coverage and frequency considerations, Delay & Throughput considerations, System considerations, Operational NGSO constellation Designs

UNIT-VI

Satellite Navigation & The Global Positioning System: Radio and Satellite Navigation, GPS Position Location principles, GPS Receivers and codes, Satellite signal acquisition, GPS Navigation Message, GPS signal levels, GPS receiver operation, GPS C/A code accuracy, Differential GPS.

Text Books:

1. Satellite Communications – Timothy Pratt, Charles Bostian& Jeremy Allnutt, WSE, Wiley Publications, 2nd Edition, 2003.
2. Satellite Communications Engineering – Wilbur L. Pritchard, Robert A Nelson & Henri G. Suyderhoud, 2nd Edition, Pearson Publications, 2003.

References:

1. Satellite Communication: Design Principles – M. Richharia, BS Publications, 2nd Edition, 2003.
2. Satellite Communication - D.C Agarwal, Khanna Publications, 5th Ed.
3. Fundamentals of Satellite Communications – K.N. Raja Rao, PHI, 2004
4. Satellite Communications – Dennis Roddy, McGraw Hill, 2nd Edition, 1996.

VIII Sem.	Bio-Medical Engineering (Professional Elective-VI)	Course Code:V18ECT35	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Explain the basics concepts of Bio-Medical Instrumentation. **[K2]**
- CO2: Explain the concepts of electrode theory, classification of Electrodes and Transducers used in Bio-Medical Applications.**[K2]**
- CO3: Explainhe Anatomy and Physiology of Cardiovascular system and Illustrate the application of Bio-Medical Instruments to measure the Physiological parameters of Cardiovascular System.**[K2]**
- CO4: Discuss the processing methods in elements used for Patient's Health care & monitoring.**[K2]**
- CO5: Explain the Principles of Diagnostic Techniques and the concepts of Bio-Telemetry.**[K2]**
- CO6: Classify different types of monitors, discuss the principles of recorders and Illustrate the methods of accident preventions i.e. Shock Hazards from different Electrical Equipment.**[K2]**

UNIT-I:

INTRODUCTIONTOBIOMEDICALINSTRUMENTATION: AgeofBiomedicalEngineering,Development of Biomedical Instrumentation, Man Instrumentation System, Components of the Man-Instrument System, Physiological System of the Body, Problems Encountered in Measuring a Living System, Sources of Bioelectric Potentials, Muscle, Bioelectric Potentials, Sources of Bioelectric Potentials, Resting and ActionPotentials,BioelectricPotentials-ECG,EEGandEMG,EvokedResponses.

UNIT-II:

ELECTRODES AND TRANSDUCERS: Introduction, Electrode Theory, Bio potential Electrodes, Examples of Electrodes, Basic Transducer Principles ,The Transducer and Transduction Principles, Active Transducers, Passive Transducers, Transducers for Biomedical Applications, Pulse Sensors, Respiration Sensor, Transducers with Digital Output.

UNIT-III:

CARDIOVASCULAR SYSTEM AND MEASUREMENTS: The Heart and Cardiovascular System, Electro Cardiography, Blood Pressure Measurement, Measurement of Blood Flow and Cardiac Output, Measurement of Heart Sounds, Plethysmography.

MEASUREMENTSINTHERESPIRATORYSYSTEM: The Physiology of The Respiratory System, Tests and Instrumentation f or the Mechanics of Breathing, Respiratory Therapy Equipment.

UNIT-IV:

PATIENTCAREANDMONITORING: ElementsofIntensive-CareMonitoring,PatientMonitoringDisplays, Diagnosis, Calibration and Repair ability of Patient-Monitoring Equipment, Other Instrumentation for Monitoring Patients, Organization of the Hospital for Patient-Care Monitoring, Pacemakers, Defibrillators.

UNIT-V:

DIAGNOSTIC TECHNIQUES AND BIO-TELEMETRY: Principles of Ultrasonic Measurement, UltrasonicImaging,UltrasonicApplicationsofTherapeuticUses,UltrasonicDiagnosis,X-RayandRadio-IsotopeInstrumentations,CATScan,EmissionComputerizedTomography,MRI,IntroductiontoBiotelemetry,Physiological Parameters Adaptable to Biotelemetry, The Components of Biotelemetry System, Implantable Units, Telemetry for ECG Measurements during Exercise, Telemetry for Emergency Patient Monitoring

UNIT-VI:

MONITORS,RECORDERSANDSHOCKHAZARDS: Bio potential Amplifiers, Monitors, Recorders, Shock Hazards and Prevention, Physiological Effects and Electrical Current, Shock Hazards from Electrical Equipment, Methods of Accident Prevention, Isolated Power Distribution System.

Text Books:

1. "Bio-Medical Electronics and Instrumentation", Onkar N.Pandey,RakeshKumar, Katson Books.
2. "Bio-Medical Instrumentation",Cromewell,Wiebell,Pfeiffer

References:

1. "HandBookofBio-MedicalInstrumentation",Khandapur.McGrawHill
2. "IntroductiontoBio-MedicalEquipmentTechnology",4th Edition,JosephJ.Carr,John M.Brown,PearsonPublications.

VIII Sem.	Wireless Sensor Networks (Professional Elective-VI)	Course Code:V18ECT36	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Explain the concepts of Wireless Sensor Networks, its Architecture. **[K2]**
- CO2: Describe the Networking Technologies**. [K2]**
- CO3: Explain the MAC Protocols**. [K2]**
- CO4: Illustrate the Routing Protocols. **[K2]**
- CO5: Describe the Transport Layer Protocols. **[K2]**
- CO6: Explain the Security Layer Protocols and Applications of WSN. **[K2]**

UNIT-I –Introduction to Wireless Sensor Networks:
Key definitions of sensor networks, Advantages of sensor Networks, Unique constraints and challenges, Driving Applications, Enabling Technologies for Wireless Sensor Networks. Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture -Sensor Network Scenarios, Gateway Concepts.

UNIT-II - Networking Technologies:
Physical Layer and Transceiver Design Considerations, Personal area networks (PANs), hidden node and exposed node problem, Topologies of PANs, MANETsand WANETs.

UNIT-III - MAC Protocols for Wireless Sensor Networks:
Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols - Contention - Based Protocols, with reservation Mechanisms, and with Scheduling Mechanisms.

UNIT-IV - Routing Protocols:
Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table–Driven Routing Protocols, On – Demand Routing Protocols, Hierarchical Routing Protocols, Proactive Routing.

UNIT-V - Transport Layer Protocols:
Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks.

UNIT- VI - Security, Platforms & Applications:
Security in Ad Hoc Wireless Networks, Network Security Requirements, Issues and Challenges in Security Provisioning; Sensor Node Hardware – Berkeley Motes, Programming Challenges; Applications - Home Automation, Smart Metering.

TEXT BOOKS:

1. Ad Hoc Wireless Networks: Architectures and Protocols, C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
2. Wireless Adhoc and Sensor Networks: Protocols, Performance and Control, JagannathanSarangapani, CRC Press.
3. Holger Karl & Andreas Willig, “Protocols and Architectures for Wireless Sensor Networks", John Wiley, 2005.

REFERENCES:

1. Wireless Sensor Networks- Technology, Protocols, and Applications, KazemSohraby, Daniel Minoli, &TaiebZnati, John Wiley, 2007.
2. Wireless Sensor Networks- Information Processing Approach, Feng Zhao & Leonidas J. Guibas, Elsevier, 2007.
3. Adhoc Mobile Wireless Networks: Protocols & Systems, C.K. Toh,1st Ed., Pearson Education.
4. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer.
5. Wireless Sensor Networks – S Anandamurugan, Lakshmi Publications.

Annexure- 02

Approved List of Open Elective- II Courses

VII Semester

S.No	Course Code	Name of the Course	Department Offered
1	V18ECTOE4	Principles of Wireless Comm.	Electronics & Communication Engineering
2	V18ECTOE5	Medical Electronics	
3	V18ECTOE6	Concepts of Embedded Systems	
4	V18CSTOE04	Operating Systems	Computer Science Engineering.
5	V18CSTOE05	Artificial Intelligence	
6	V18CSTOE06	Java Programming	
7	V18EEOE4	Non-Conventional Energy Sources	Electrical & Electronics Engineering
8	V18EEOE5	Electrical Engineering Materials	
9	V18EEOE6	Servicing of Electrical Appliances	
10	V18MEOE4	Computer Aided Design	Mechanical Engineering
11	V18MEOE5	Condition Monitoring & Machine learning	
12	V18CEOE03	Environmental Pollution and Control	Civil Engineering
13	V18CEOE04	Disaster Management	

Approved List of Open Elective- III Courses

VIII Semester

S.No	Course Code	Name of the Course	Department Offered
1	V18ECTOE7	Fundamentals of Digital Image & Video Processing	Electronics & Communication Engineering
2	V18ECTOE8	Embedded RTOS	
3	V18ECTOE9	Principles of Digital TV Engg	
4	V18CSTOE07	Software Testing Methodologies	Computer Science Engineering.
5	V18CSTOE08	Cyber Security	
6	V18CSTOE09	Computer Graphics	
7	V18EEOE7	Energy Storage Systems	Electrical & Electronics Engineering
8	V18EEOE8	Basics of Electrical Power Generation	
9	V18EEOE9	Industrial Automation	
10	V18MEOE6	Power Plant Engineering	Mechanical Engineering
11	V18MEOE7	Mechatronics	
12	V18CEOE05	Solid Waste Management	Civil Engineering
13	V18CEOE06	Water Quality and Conservation	

VII Sem.	Principles of Wireless Comm. (Open Elective-II)	Course Code:V18ECTOE4	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

CO1: Discuss the cellular system evolution of mobile radio systems **[K2]**
CO2: Illustrate the basic cellular concepts. **[K2]**
CO3: Explain the Various Propagation models. **[K2]**
CO4: Discuss the need of modulation, diversity and equalization in cellular & Mobile Communication. **[K2]**
CO5: Demonstrate the knowledge about GSM architecture, multiple access schemes like FDMA,TDMA, CDMA. **[K2]**
CO6: Summarize the concepts of upcoming technologies like 3G, 4G etc. **[K2]**

UNIT-I: Introduction of Wireless Communication
History and evolution of mobile radio systems: Types of mobile wireless services/systems- Cellular, WLL, Paging, Satellite systems, Future trends in personal wireless systems.

UNIT-II: Cellular Concepts and System Design Fundamentals
Cellular concept and frequency reuse, channel assignment, handoff strategies, Interference and system capacity, Trunking and GOS, cell splitting,cell sectoring.

UNIT-III: Mobile radio Propagation Models

Radio wave propagation issues in personal wireless systems, Propagation models, Multipath fading, parameters of mobile multipath channels and Antenna systems in mobile radio.

UNIT-IV: Overview analog and digital modulation techniques
Need For Modulation. Different Analog and Digital modulation techniques used in Cellular and mobile communication systems.

UNIT-V DIGITAL CELLULAR NETWORKS: GSM architecture, GSM Services, multiple access schemes; FDMA, TDMA, CDMA, OFDMA;

UNIT-VI Higher Generation Cellular Standards: 3G System architecture (UMTS), 4G System Architecture, Introduction to 5G.

Text Books

1. Theodore S. Rappaport, "wireless communications Principles and Practices", PHI, 2005
2. Jochen Schiller, "Mobile Communications", Pearson Education, second edition, 2009.

Reference Book

1. Lee W.C.Y, "Mobile communication Engineering
2. Theory and Applications", 2/e McGraw-Hill,New York, 2003
3. Andreas F. Molisch, "Wideband Wireless Digital Communication", Pearson Education 2001.
4. Blake, "Wireless Communication Technologies," Thomson Delmer, 2003

VII Sem.	Medical Electronics (Open Elective-II)	Course Code:V18ECTOE5	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Explain the basics concepts of Bio-Medical Instrumentation.**[K2]**
- CO2: Explain the concepts of electrode theory, classification of Electrodes and Transducers used in Bio-Medical Applications.**[K2]**
- CO3: Explainthe Anatomy and Physiology of Cardiovascular system and Illustrate the application of Bio-Medical Instruments to measure the Physiological Parameters of Cardiovascular System. **[K2]**
- CO4: Discuss the elements used for Patient's Health care & monitoring.**[K2]**
- CO5: Explain the Principles of Diagnostic Techniques and the concepts of Bio-Telemetry.**[K2]**
- CO6: Classify different types of monitors, discuss the principles of recorders and Illustrate the methods of accident preventions.**[K2]**

UNIT-I:

INTRODUCTION TO BIOMEDICAL INSTRUMENTATION: Age of Biomedical Engineering, Development of Biomedical Instrumentation, Man Instrumentation System, Components of the Man-Instrument System, Physiological System of the Body, Problems Encountered in Measuring a Living System, Sources of Bioelectric Potentials, Muscle, Bioelectric Potentials, Sources of Bioelectric Potentials, Resting and Action Potentials, Bioelectric Potentials-ECG, EEG and EMG,

UNIT-II:

ELECTRODES AND TRANSDUCERS: Introduction, Electrode Theory, Biopotential Electrodes, Examples of Electrodes, Basic Transducer Principles, Active Transducers, Passive Transducers, Transducers for Biomedical Applications, Pulse Sensors, Respiration Sensor, Transducers with Digital Output.

UNIT-III:

CARDIOVASCULAR SYSTEM AND MEASUREMENTS: The Heart and Cardiovascular System, ElectroCardiography, Blood Pressure Measurement, Measurement of Blood Flow and Cardiac Output, Measurement of Heart Sounds, Plethysmography.

UNIT-IV:

PATIENTCAREANDMONITORING: ElementsofIntensive-CareMonitoring,PatientMonitoringDisplays, Diagnosis, Calibration and Repair ability of Patient-Monitoring Equipment, Other Instrumentation for Monitoring Patients, Organization of the Hospital for Patient-Care Monitoring, Pacemakers, Defibrillators.

UNIT-V:

DIAGNOSTIC TECHNIQUES AND BIO-TELEMETRY: Principles of Ultrasonic Measurement, UltrasonicImaging,UltrasonicApplicationsofTherapeuticUses,UltrasonicDiagnosis,X-RayandRadio-IsotopeInstrumentations,CATScan,EmissionComputerizedTomography,MRI,IntroductiontoBiotelemetry,Physiological Parameters Adaptable to Biotelemetry, The Components of Biotelemetry System, Implantable Units, Telemetry for ECG Measurements during Exercise, Telemetry for Emergency Patient Monitoring.

UNIT-VI:

MONITORS, RECORDERS AND SHOCK HAZARDS: Bio potential Amplifiers, Monitors, Recorders, Shock Hazards and Prevention, Physiological Effects and Electrical Current, Shock Hazards from Electrical Equipment, Methods of Accident Prevention.

Text Books:

1."Bio-MedicalElectronicsand Instrumentation", Onkar N.Pandey,RakeshKumar, Katson Books.
2."Bio-Medical Instrumentation", Cromewell, Wiebell,Pfeiffer

References:

1."Hand Book of Bio-Medical Instrumentation", Khandapur.McGrawHill
2."IntroductiontoBio-MedicalEquipmentTechnology",4th Edition,JosephJ.Carr,John M.Brown, Pearson Publications.

VII Sem.	Concepts of Embedded Systems (Open Elective-II)	Course Code:V18ECTOE6	L	T	P	C
			3	0	0	3

Syllabus Details

COs	Course outcomes
CO1	Describe the Basic Concepts of embedded systems- **(K2).**
CO2	Describe the characteristics of Embedded Systems - **(K2)**
CO3	Explain the Architecture and Pin Description of 8051- **(K2)**
CO4	Explain various Addressing Modes and Instructions of 8051- **(K2)**
CO5	Discuss the various Interrupts , Modes of Timers/Counters in 8051**-(K2)**
CO6	Discuss the fundamentals of RTOS based embedded firmware design - **(K2)**

UNIT-I - INTRODUCTION TO EMBEDDED SYSTEMS:

Introduction to Embedded Systems, Embedded Systems vs. General Computing Systems, Classification of Embedded systems, Major application areas of embedded systems, Purpose of embedded Systems, The Typical embedded system - core of the embedded system, Difference between RISC and CISC, Types of Memories.

UNIT-II - CHARACTERISTICS OF EMBEDDED SYSTEM:

Characteristics of an embedded system, Quality attributes of embedded systems, Application-specific and Domain-Specific examples of an embedded system.

UNIT-III-8051 Micro Controller – Architecture, Pin Description

Introduction, 8051 Architecture, Registers in 8051, Pin Diagram – Description, Parallel I/O Ports and Memory Organization

UNIT-IV - 8051 Micro Controller – Addressing Modes and Instructions:

8051 Addressing Modes, 8051 Instruction Set, Instructions and Sample Programs, Stack Pointer

UNIT-V - 8051 Micro Controller – Interrupts, Timer/ Counter:

Interrupts in 8051, Timers and Counters, Timer/ Counter Modes, Serial Communication – Modes

UNIT-VI- REAL TIME OPERATING SYSTEM:

Operating System basics, Types of operating systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling, Inter Task communication.

Text Books:

1. Embedded Systems-By Shibu. K.V-Tata McGraw Hill Education Private Limited,2013.
2. Micro Controllers [Theory and Applications] – Ajay V Deshmukh – Tata McGraw-Hill Education Private Limited,2012

References:

1. The 8051 Micro Controller- Kenneth Ayala – CENGAGE- 3rd Edition
2. Embedded/Real Time Systems by KVKK Prasad by Dreamtech Publication

VIII Sem.	Fundamentals of Digital Image & Video Processing (Open Elective-III)	Course Code:V18ECTOE7	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Analyse Image transforms for various Image processing operations**(K4)**
- CO2: Examine Spatial & frequency domain filtering like smoothing & sharpening Operations on Images**(K4)**
- CO3: Estimate Image degradation functions and Analyze various Image Restoration Techniques on Images**(K4)**
- CO4: Analyze various Image segmentation techniques**(K4)**
- CO5: Describe various Image compression techniques**(K3)**
- CO6: Explain basic concepts regarding to motion estimation, video filtering and Video standards.**(K2)**

UNIT-I

IMAGE FUNDAMENTALS & TRANSFORMS: Fundamental steps in digital image processing, components of an image processing system, image sensing and acquisition, image sampling and quantization. Two dimensional orthogonal transforms: DFT, WHT, Haar transform, DCT and DST

UNIT-II

Intensity Transformations, Spatial Filtering and frequency domain filtering: Some basic intensity transformation functions, histogram processing, fundamentals of spatial filtering, smoothing spatial filters, sharpening spatial filters, `Image smoothing and sharpening in frequency domain filtering

UNIT-III

IMAGE RESTORATION: Degradation Models, Linear Position –Invariant Degradations, Estimating the degradation function, inverse filtering, Minimum mean square error (Wiener) filtering and geometric mean filter.

UNIT-IV

IMAGESEGMENTATION: Pixelclassification,Bi-levelThresholding,Multi-levelThresholding,AdaptiveThresholding,Spectral& spatial classification, Edge detection, Hough transform, Region growing.

UNIT-V

IMAGE COMPRESSION: Compression models, Huffman Coding, Arithmetic coding, Bit plane coding, run length coding, Lossy compression: Transform coding, Image compression standards.

UNIT-VI

VIDEO PROCESSING: Representation of Digital Video, Spatio-temporal sampling, Motion Estimation. Video Filtering, Video Compression, Video coding standards.

Text Books:

1. R.C.Gonzalez,R.E.Woods,"DigitalImageProcessing",PearsonEducation. 2nd edition,2002
2. M.Tekalp,"DigitalVideoProcessing",Prentice-Hall,1995

Reference Books:

1. AnilK.Jain,"FundamentalsofDigitalImageProcessing",PrenticeHallofIndia,9th Edition, Indian Reprint,2002.
2. B.Chanda, D.Dutta Majumder,"Digital ImageProcessingandAnalysis",PHI,2009.
3. Bovik,"HandbookofImage&Videoprocessing",AcademicPress,2000.
4. Khalid Sayood, Introduction to data compression ,third edition, The Morgan Kaufmann publishers,2005

VIII Sem.	Embedded RTOS (Open Elective-III)	Course Code:V18ECTOE8	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1: Describe the basics of Real time OS. **[K2]**
- CO2: Explain the tasks, Interrupts, Security. **[K2]**
- CO3: Describe the basics of µCOS-II RTOS. **[K2]**
- CO4: Describe the basics of µCOS-II RTOS. **[K2]**
- CO5: Illustrate the mechanism of target image creation and porting. **[K2]**
- CO6: Explain the Application of RTOS. **[K2]**

UNIT-I: Introduction
OS Basics, Task, Process, Threads, Multiprocessing & Multitasking, Process Management, Timer Functions, Event Functions, Memory Management, Device, File and IO Systems Management, Interrupt Routines in RTOS Environment and Handling of Interrupt Source Calls.

UNIT-II: RTOS
Basic Design Using an RTOS, RTOS Task Scheduling Models, Interrupt Latency and Response of the Tasks as Performance Metrics, OS Security Issues. Basic Functions and Types of RTOS.

UNIT-III: RTOS µCOS-II
Introduction, Task Service, Task Scheduling, Memory Allocation, IPC – Semaphore, Mailbox, Queue, Interrupt Handling.

UNIT-IV: RTOS Vx Works
Introduction, Task Service, Task Scheduling, Memory Allocation, IPC – Semaphore, Mailbox, Queue, Interrupt Handling.

UNIT-V: Embedded OS & Target Image Creation
Off-The-Shelf Operating Systems, Embedded OS, Handheld OS, Operating System Software, Target Image Creation for Window XP Embedded, Porting RTOS on a Micro Controller based Development Board.

UNIT-VI: Program Modeling – Case Studies
Case study of embedded system design and coding for an Automatic Chocolate Vending Machine (ACVM) Using µCOS-II RTOS, Case study of digital camera hardware and software architecture, Using RTOS Vx Works, Case Study of Embedded System for an Adaptive Cruise Control (ACC) System in Car, Case Study of Embedded System of Mobile Phone Software for Key Inputs.

TEXT BOOKS:

1. Shibu K V: "Introduction to Embedded Systems", Tata McGraw Hill Publications, Second Edition.
2. Dr. K.V.K.K. Prasad: "Embedded/Real-Time Systems", Dream Tech Publications, Black pad.
3. Raj Kamal: "Embedded Systems-Architecture, Programming and Design", Tata McGraw Hill Publications, Second Edition.

REFERENCES:

1. Labrosse, "Embedding system building blocks ", CMP publishers.
2. Rob Williams," Real time Systems Development", Butterworth Heinemann Publications.

VIII Sem.	Principles of Digital TV Engineering (Open Elective-III)	Course Code:V18ECTOE9	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

CO1:	Illustrate the fundamentals of television engineering	**[K2]**
CO2:	Explain about TV signal transmission	**[K2]**
CO3:	Explain the colour TV fundamentals	**[K2]**
CO4:	Classify Digital TV transmission standards	**[K2]**
CO5:	Explain the operation of Digital TV receiver	**[K2]**
CO6:	Describe the working of LCD and Plasma screens	**[K2]**

UNIT-I

Introduction: TV transmitter and receivers, synchronization **Television Pictures**: Geometric form and aspect ratio, image continuity, interlaced scanning, picture resolution

UNIT-II

Composite video signal: Horizontal and vertical sync details **TV Signal Transmission:** VSB transmission, standard channel BW, TV transmitter

UNIT-III

Colour Television: Perception of brightness and colours, additive colour mixing, video signals for colours, luminance signal, colour difference signals, encoding of colour difference signals, formation of chrominance signals, PAL encoder, PAL colour receiver

UNIT-IV

Digital Television Transmission Standards: ATSC terrestrial transmission standard, vestigial sideband modulation, DVB -T transmission standard, ISDB-T transmission standard

UNIT-V

Digital Television: Digital Satellite Television, Direct to Home Satellite Television, Digital TV Receiver, Merits of Digital TV Receivers

UNIT-VI

LCD Screens: LCD Technology, LCD Matrix types and operation, LCD Screens for Television, LCD color receiver

Plasma Screens: Plasma and conduction of charge, Plasma TV Screens, Plasma Color Receiver

Text Books:

1. Television engineering and video systems – R G Gupta, Tata McGraw Hill Publishers.

2. Television and Video Engineering – A.M.Dhake, 2nd Edition, Tata McGraw Hill Publishers.

3. Modern Television Practice: Transmission, Reception and Applications- R RGulati, 4th revised edition, New Age International Publishers.

4. Fundamentals of Digital Television Transmission- Gerald W. Collins, John Wiley & Sons.

References

1. Basic Television and Video Systems – Bernard Grob, McGrawHill Publishers.

2. Monochrome and Colour Television - R RGulati, New Age International Publishers.

3. Colour Television, Theory and Practice - S.P.Bali, Tata McGraw-Hill Publishers.

Approved Course Structure & Syllabus

COURSE STRUCTURE

(For V20 Regulation)

ECE

V20 Regulation

Semester III (Second Year)

Sl. No.	Course Category	Course Code	Course Title	Hours per Week			Credits
1.	Basic Science Courses		Mathematics-III **(M-III)**	3	0	0	3
2.	Professional Core Course	V20ECT02	Electronic Devices, Circuits & Analysis **(EDCA)**	3	0	0	3
3.	Professional Core Courses		Probability Theory Stochastic Process **(PTSP)**	3	0	0	3
4.	Professional Core Courses	V20ECT04	Network Theory **(NT)**	3	0	0	3
5.	Professional Core Courses	V20ECT05	Signals & Systems **(SS)**	3	0	0	3
6.	Professional Core Courses (LAB)	V20ECL01	Electronic Devices, Circuits & Analysis Lab **(EDCA LAB)**	0	0	3	1.5
7.	Professional Core Courses (LAB)	V20ECL02	Signals & Systems Lab **(SS LAB)**	0	0	3	1.5
8.	Professional Core Courses (LAB)	V20CSL31	Data Structures Lab **(DS LAB)**	0	0	3	1.5
9	**Skill Oriented Course***	V20ECSOC01	Certificate course being offered by industries/ professional bodies/ APSSDC or any other accredited bodies	**1**	**0**	**2**	**2**
10	Mandatory Course (AICTE suggested)	V20ENT02	Professional Communication Skills **(PCS-I)**	2	0	0	0
						Total Credits	**21.5**

Semester IV (Second Year)

Sl. No.	Course Category	Course Code	Course Title	Hours			Credits
				L	**T**	**P**	
1.	Engineering Science Courses	V20EET11	Control Systems **(CS)**	3	0	0	3
2.	Basic Science Course/Prof Core Course	V20ECT07	Analog & Digital Communication **(ADC)**	3	0	0	3
3.	Professional Core Courses	V20ECT08	Digital IC Applications **(DICA)**	3	0	0	3
4.	Professional Core Courses	V20ECT09	Electro Magnetic Waves & Transmission Lines **(EMTL)**	3	0	0	3
5.	Humanities and Social Sciences		Managerial Economics & Financial Analysis (**MEFA)**	3	0	0	3
6.	Engineering Science Courses/Prof Core (Interdisciplinary) (LAB)	V20CSL33	Python Programming Lab	0	0	3	1.5
7.	Professional Core Courses (LAB)	V20ECL04	Analog & Digital Communication Lab **(ADC LAB)**	0	0	3	1.5
8.	Professional Core Courses (LAB)	V20ECL05	Digital IC Applications Lab **(DICA LAB)**	0	0	3	1.5
9	**Skill Oriented Course***	V20ECSOC02	Certificate course being offered by industries/ professional bodies/ APSSDC or any other accredited bodies	**1**	**0**	**2**	**2**
10	Mandatory Course (AICTE suggested)	V20ENT03	Professional Communication Skills **(PCS-II)**	2	0	0	0
						Total Credits	**21.5**

	Internship 2 Months (Mandatory) during Summer vacation				
	Honors/Minor Courses (The Hours Distribution can be 3-0-2 or 3-1-0 also)	**4**	0	**0**	**4**

***Skill Oriented Course:**

The Student shall be given an option to choose either the skill courses being offered by the college or to choose a certificate course being offered by industries/ professional bodies/ APSSDC or any other accredited bodies as approved by the concerned BoS.

List of Skill Oriented Courses:

S. No	Name of the Proposed Course
1	PCB Design
2	Programming in Scilab
3	Programming with Arduino
4	Circuit Design & Simulation using Multisim
5	Concepts of Embedded systems
6	Internet of Things
7	Robotics
8	Hands on Graphical Programming Using Labview

III Semester
SYLLABUS

III Sem.	Electronic Devices, Circuits & Analysis	Course Code:V20ECT02	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of this course, the students will be able to:

- CO1: Explain the formation of p-n Junction, Discuss special semi-conductor Diodes & Explain the working principle of rectifiers with and without filters With relevant expressions and necessary comparisons**[K2]**
- CO2: Understand the construction, principle of operation of transistors, BJT and FET with their V-I characteristics in different configurations.**[K2]**
- CO3: Explain the need of transistor biasing, various biasing techniques for BJT. **[K2]**
- CO4: Analyze small signal low frequency transistor amplifier circuits using BJT In Single & Multistage.**[K2]**
- CO5: Explain the operation & Analysis of Feedback and Power amplifiers.**[K2]**

UNIT-I: Junction diode characteristics: p-n junction diode, energy band diagram of PN junction Diode, current components in PN junction Diode, law of junction, derivation of diode equation, V-I Characteristics, Diode resistance, Diode capacitance. Zener Diode, Breakdown mechanisms, UJT, Construction and characteristics

Rectifiers and Filters: Rectifier Classification, characteristics of rectifiers, Filters- Capacitor filter, Inductor filter, derivation for ripple factor in each case.

UNIT- II: Transistor Characteristics: BJT: Junction transistor, transistor current components, Transistor equation, Characteristics of transistor in Common Base, Common Emitter and Common Collector configurations, Early Effect.

FET: Comparison between BJT and FET.FET types, construction, operation, characteristics, MOSFET- types, construction, operation, characteristics.

UNIT- III: Transistor Biasing &Thermal Stabilization

BJT: Need for biasing, operating point, Load line analysis, BJT biasing- methods, fixed bias, collector to base bias, self-bias, Stabilization against variations in VBE, Ic, and β,Stability factors(S, S", S""),Bias compensation.

UNIT-IV: Small Signal Analysis of BJT

Two port network, Transistor hybrid model, determination of h- parameters, Generalized Analysis of CB, CE and CC amplifiers using exact and approximate analysis,Low frequency analysis of Cascade and Cascode amplifiers.

UNIT-V: Feedback Amplifiers, Oscillators & Power Amplifiers

Feedback principle and concept, types of feedback, classification of amplifiers, feedback topologies Generalized analysis of Voltage series, current series, voltage shunt, current shunt feedback amplifiers,

Oscillators: Basic concept, Barkhausen criterion, RC oscillators (phase shift, Wien bridge), LC oscillators (Hartley, Colpitts)various classes of operation (Class A, B, AB), power efficiency calculations.

Text Books:

1. Electronic Devices and Circuits- J. Millman, C. Halkias,TMH.
2. Integrated Electronics- Jacob Millman, C. Halkies, C.D.Parikh,TMH.
3. Electronic Circuit Analysis - B.V.Rao, K.R.Rajeswari, P.C.R.Pantulu, K.B.R.Murthy, Pearson Publications

References:

1. Electronic Devices and Circuits Theory – Robert L. Boylestad and Louis Nashelsky, Pearson/Prentice Hall.
2. ElectronicCircuitAnalysisandDesign–Donald A.Neaman,McGrawHill.

III Sem.	Probability Theory & Stochastic Processes	Course Code:	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of this course, the students will be able to:

CO-1: Explain basic concepts of probability theory through Sets and Relative Frequency **(K2)**

CO-2: Explain the concept of a random variable, functions based on random variable like Distribution and density functions (**K2)**

CO-3: Compute the expected value, moments on one random variable **(K3)**

CO-4: Illustrate the concepts of joint distribution & density functions on multiple random Variables**(K3)**

CO-5: Compute the Temporal and Spectral characteristics of stochastic processes **(K3)**

UNIT I PROBABILITY : Probability introduced through Sets and Relative Frequency: Experiments and Sample Spaces, Discrete and Continuous Sample Spaces, Events, Probability Definitions and Axioms, Mathematical Model of Experiments, Probability as a Relative Frequency, Joint Probability, Conditional Probability, Total Probability, Bayes Theorem, Independent Events

UNIT II THE RANDOM VARIABLE: Definition of a random variable, Discrete, continuous and mixed random Variables. Distribution & density functions and its properties of a random variable. Binomial, Poisson, Uniform, Gaussian, Exponential and Rayleigh random variables. Conditional distribution and density functions and its properties.

UNIT III OPERATION ON ONE RANDOM VARIABLE – EXPECTATIONS : Introduction, expected value of a random variable, function of a random variable, moments about the origin, central moments, variance, characteristic function, moment generating function, transformations of a random variable: Monotonic transformations for a continuous random variable

UNIT IV MULTIPLE RANDOM VARIABLES : Vector random variables, joint distribution function, properties of joint distribution, marginal distribution functions, conditional distribution and density, statistical independence, sum of two random variables, sum of several random variables, central limit theorem: unequal distribution, equal distributions.
OPERATIONS ON MULTIPLE RANDOM VARIABLES: Joint moments about the origin, joint central moments, joint characteristic and moment generating functions.

UNIT V RANDOM PROCESSES – TEMPORAL CHARACTERISTICS: The random process concept, classification of processes, deterministic and nondeterministic processes, distribution and density functions, concept of Stationarity and statistical independence. First-order stationary processes, second-order and wide-sense Stationarity, nth-order and strict-sense Stationarity, time averages and Ergodicity, autocorrelation function and its properties, cross-correlation function and its properties, covariance functions.
SPECTRAL CHARACTERISTICS: The power density spectrum: properties, relationship between power density spectrum and autocorrelation function, the cross-power density spectrum, properties, relationship between cross-power density spectrum and cross-correlation function.

TEXT BOOKS:

1. Probability, Random Variables & Random Signal Principles, Peyton Z. Peebles, TMH, 4th Edition, 2001.
2. Probability, Random Variables and Stochastic Processes, Athanasios Papoulis and S. UnniKrishnaPillai, PHI, 4th Edition, 2002.
3. Probability Theory and Stochastic Processes, Y. Mallikarjuna Reddy, 4th Edition, Universities Press

Reference Books:

1. Probability Theory and Stochastic Processes – B. PrabhakaraRao, BS Publications
2. Probability and Random Processes with Applications to Signal Processing, Henry Stark And John W. Woods, Pearson Education, 3rd Edition.
3. Schaum's Outline of Probability, Random Variables, and Random Processes.
4. An Introduction to Random Signals and Communication Theory, B.P. Lathi, International Textbook, 1968.
5. Random Process – Ludeman, John Wiley
6. Probability Theory and Random Processes, P. Ramesh Babu, McGrawHill, 2015.

III Sem.	Network Theory	Course Code: V20ECT04	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of this course, the students will be able to:

- CO1: Apply network theorems to solve the electrical circuits. **[K3]**
- CO2: Describe the steady state analysis of RLC circuits. **[K2]**
- CO3: Analyze the resonance circuits. **[K4]**
- CO4: Solve the two port network parameters. **[K3]**
- CO5: Explain RLC transient circuits. **[K2]**

UNIT – I - ELECTRICAL CIRCUITS FUNDEMENTALS AND THEOREMS:
Electric circuits: Network elements classification, Source transformation, Kirchhoff's laws, Mesh analysis and Nodal analysis problem solving with resistances only including dependent sources. **Network theorems:** Thevenin's, Norton's, Milliman's, Reciprocity, Compensation, Substitution, Superposition, Max Power Transfer, - Problem solving using dependent sources also.

UNIT – II - STEADY STATE ANALYSIS OF A.C CIRCUITS
Response to sinusoidal excitation: - pure resistance, pure inductance, pure capacitance, series R-L, R-C, R-L-C circuits, parallel R-L, R-C, R-L-C circuits. Impedance concept, phase angle, problem solving for R-L, R-C and R-L-C circuits using mesh and nodal analysis.

UNIT-III RESONANCE
Series Resonance: resonance frequency, impedance, current, power factor, bandwidth, cutoff frequencies &Q-factor.
Parallel Resonance: resonance frequency, impedance, current, power factor, bandwidth, cutoff frequencies Q-factor. Comparison of series and parallel resonance circuits and solving problems.

UNIT – IV - TWO-PORT NETWORKS
Z-parameters, Y-parameters, Transmission parameters, h-parameters, series connection, Parallel connection, Cascade connection of two port networks. Relationship of two port networks, problem solving

UNIT – V – TRANSIENTS
Initial and final condition in capacitor and inductor, Definition of time constants, R-L, R-C, R-L-C circuits with DC excitation, problem solving using R-L-C elements with DC excitation. Solutions using Laplace transform method.

TEXT BOOKS:
1. Electric Circuit Analysis by Hayt and Kimmarle, TMH.
2. Network Analysis by Van-Valkenberg, PHI.
3. Circuit Theory (Analysis and Synthesis) by ABHIJIT Chakrabarti, DhanpatRai&Co.

REFERENCES:
1. Basic Circuit Analysis by DR Cunninghan, Jaico Publishers.
2. Network Analysis and Filter Design by Chadha, Umesh Publications.
3. Circuits & Network Analysis & Synthesis - A.Sudhakar&Shyam MohanS.Pillai, TMH.

III Sem.	Signals & Systems	Course Code: V20ECT05	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of this course, the students will be able to:

CO1 Classify the signals and various operations on signals.**[K2]**
CO2 Determine the response of LTI system to any arbitrary input signal using convolution**[K2]**
CO3 Analyze the spectral characteristics of signals using Fourier series and Fourier transforms.**[K3]**
CO4 Apply the various sampling techniques on continuous time signals.**[K3]**
CO5 Applytheconceptsof Laplacetransform/Z-transformtoanalyzecontinuous-time/discrete-timesignalsincomplexplane. **[K3]**

UNIT-I

SignalsandSystems: Continuous-timeandDiscrete-timesignals,Transformationsoftheindependentvariable,Exponential and Sinusoidal signals, the unit impulse and unit step functions, Continuous-time and Discrete-time systems and Basic System properties.

UNIT-II

Linear Time Invariant Systems (LTI systems): Discrete-time LTI systems, the convolution sum,ContinuoustimeLTIsystems,theconvolutionIntegral,PropertiesofLinearTime-InvariantSystems.

UNIT-III

Fourier series: Fourier series representation of Continuous-time periodic signals, Convergence of the Fourier series, Properties of Continuous time Fourier series.
Fourier transform: Representation of periodic signals: The Continuous-time Fourier transform, The Fourier transform for periodic signals, Properties of the continuous time Fourier transform.

UNIT-IV

Sampling Theorem: Introduction, Sampling theorem for band limited signals- explanation, NY Quist rate, Reconstruction of a signal from its samples using Interpolation, The effect of under sampling: Aliasing, sampling techniques- impulse, natural and flat top sampling.

UNIT-V

Analysis of Continuous time and discrete time signals using Laplace Transform and Z Transform: The Laplace Transform:The Region of convergence for Laplace transforms, the Inverse Laplace transform, Properties of the Laplace transform. TheZ-Transform: The Region of Convergence for the Z-transform, The InverseZ-transform,Propertiesofthe Z-transform.

TEXT BOOKS:

1. Signals and Systems, A.V. Oppenheim and A.S. Will sky with S. H. Nawab, Second Edition, and PHI Private limited.
2. Signals and Systems, Second Edition, S. Haykin and B. Van Veen, John Wiley & Sons.
3. B.P. Lathi, “Principles of Linear Systems and Signals”, Second Edition, Oxford, 2009.

REFERENCES:

1. R.E.Zeimer, W.H.Tranter and R.D.Fannin, “Signals & Systems - Continuous and Discrete”, Pearson, 2007.
2. John Alan Stuller, “An Introduction to Signals and Systems”, Thomson, 2007. 40.

3.M.J.Roberts, “Signals & Systems Analysis using Transform Methods & MATLAB”, Tata McGraw

III Sem.	Electronic Devices, Circuits & Analysis Lab	Course Code: V20ECL01	L	T	P	C
			0	0	3	1.5

Syllabus Details

Course Outcomes: After Successful completion of this course, the students will be able to:

CO1-Identify,Test and Describe the specifications of various components**.[K2]**

CO2-Interpret the Characteristics of various Semiconductor Devices.**[K2]**

CO3-Sketch the Regulation Characteristics of Zener Diode.**[K3]**

CO4-Examine the Performance of Rectifiers with and without Filters.**[K3]**

CO5-Sketch the Frequency Response of Amplifiers and Compute Bandwidth.**[K3]**

CO6- Construct different RC and LC oscillators using BJT based on the Frequency range.**[K3]**

PART A ELECTRONIC WORKSHOP PRACTICE

1. Identification, Specifications, Testing of R, L, C Components (Colour Codes), Potentiometers, Coils, Gang Condensers, Relays, Bread Boards.
2. Identification, Specifications and Testing of Active Devices, Diodes, BJTs, JFETs, LEDs, UJT.
3. Study and operation of Ammeters, Voltmeters, Transformers, Analog and digital Multimeter, Function generator, Regulated power supply and CRO.

PART B: List of Experiments

1. PN Junction diode characteristics
2. Zener diode characteristics
3. Rectifier(without and with c-filters)
   - Part-A Half- wave Rectifier
   - Part-B Full- wave Rectifier
4. BJT characteristics (CB Configuration Input & Output characteristics)
5. BJT characteristics (CE Configuration Input & Output characteristics)
6. FET Characteristics (CS Configuration Drain&Transfer Characteristics
7. BJT-CE Amplifier
8. RC Phase Shift Oscillator
9. Colpit's Oscillator
10. Complementary Symmetry Class B Power Amplifier

Equipment required for EDC&Analysis Laboratory

1. Ammeters (Analog or Digital)
2. Voltmeters (Analog or Digital)
3. Active & Passive Electronic Components
4. Regulated Power supplies
5. Cathode Ray Oscilloscopes
6. Analog/ Digital function Generators
7. Digital multimeter
8. Decade resistance Boxes/Rheostats
9. Bread Boards

III Sem.	Signals & Systems Lab	Course Code: V20ECL02	L	T	P	C
			0	0	3	1.5

Syllabus Details

Course Outcomes: After Successful completion of this course, the students

Will be able to:

CO1. Understand basics of MATLAB syntax, functions and programming. **[K2]**

CO2. Describe continuous-time and discrete time signals and systems. **[K2]**

CO3. Analyze the spectral characteristics of signals using Fourier analysis. **[K4]**

CO4. Analyze the systems using Laplace transform and Z-transform. **[K4]**

LIST OF EXPERIMENTS:

1. Basic operations on matrices.
2. Generation on various signals and Sequences (periodic and aperiodic), such as unit impulse, Unit step, square, saw tooth, triangular, sinusoidal, ramp, sinc.
3. Operations on signals and sequences such as addition, multiplication, scaling, shifting, Folding, computation of energy and average power.
4. Finding the even and odd parts of signal/sequence and real and imaginary part of signal.
5. Convolution between signals and sequences.
6. Auto correlation and cross correlation between signals and sequences.
7. Verification of linearity and time invariance properties of a given continuous /discrete System.
8. Computation of unit sample, unit step and sinusoidal response of the given LTI system and Verifying its physical Reliability and stability properties.
9. Gibbs phenomenon.
10. Finding the Fourier transform of a given signal and plotting its magnitude and phase Spectrum.
11. Waveform synthesis using Laplace Transform.
12. Locating the zeros and poles and plotting the pole zero maps in s-plane and z-plane for the Given transfer function.

IV Semester
SYLLABUS

IV Sem.	Control Systems	Course Code: V20EET11	L	T	P	C
			3	0	0	3

Course Outcomes

After successful completion of this course, students will be able to

CO No.	Course Outcome	Knowledge Level
CO1	Determine the mathematical modelling of physical systems	(K3)
CO2	Calculation of Time Domain Specification of first and second order systems and understand the effect of Controllers	(K3)
CO3	Investigate the stability of closed loop systems using Routh's stability criterion and root locus method.	(K3)
CO4	Find the stability of control systems using frequency response approaches.	(K3)
CO5	Analyze physical systems using state space approach.	(K4)

Unit – I: Mathematical Modeling of Control Systems

Classification of control systems, Open Loop and closed loop control systems and their differences, Feed-Back Characteristics, transfer function of linear system, Differential equations of electrical networks, Translational and Rotational mechanical systems, Transfer Function of DC Servo motor - AC Servo motor- Synchro, transmitter and receiver - Block diagram algebra – Representation by Signal flow graph - Reduction using Mason's gain formula.

Unit-II: Time Response Analysis

Standard test signals - Time response of first and second order systems - Time domain specifications - Steady state errors and error constants – Effects of various controllers

Unit –III: Stability And Root Locus Technique

The concept of stability – Routh's stability criterion –limitations of Routh's stability –Root locus concept - construction of root loci

Unit–IV: Frequency Response Analysis

Introduction to Frequency domain specifications-Bode diagrams- transfer function from the Bode Diagram-Phase margin and Gain margin-Stability Analysis from Bode Plots, Polar Plots, Nyquist Stability criterion. Effects of various controllers.

Unit–V: State Space Analysis of LTI Systems

Concepts of state, state variables and state model, state space representation of transfer function, Diagonalization-Solving the time invariant state equations- State Transition Matrix and it's Properties – Concepts of Controllability and Observability.

Text Books:

1. Control Systems principles and design, M. Gopal, Tata McGraw Hill education Pvt Ltd., 4th Edition, 2014.
2. Automatic control systems, Benjamin C. Kuo, Prentice Hall of India,2nd Edition, 2014.

Reference Books:

1. Modern Control Engineering, Kotsuhiko Ogata, Prentice Hall of India, 2002.
2. Control Systems, ManikDhanesh N, Cengage Publications, 2012.
3. Control Systems Engineering, I.J.Nagarath and M.Gopal, Newage International Publications, 5th Edition, 2007.
4. Control Systems Engineering, S.Palani, Tata McGraw Hill Publications, 2009.

IV Sem.	Analog & Digital Communication	Course Code:	V20ECT07	L	T	P	C
				3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of this course, the students Will be able to:

- CO1:Explainthespectralcharacteristics,generationanddetection Techniques of Amplitude modulation techniques**(K2)**
- CO2: Explain the spectral characteristics, generation and Detection techniques of angle modulation techniques**(K2)**
- CO3:Illustrate different types of noise and predict its effect on Analog communication Systems.**(K3)**
- CO4: Describe the generation and detection methods of various digital Modulation schemes.**(K2)**
- CO5: Analyze the concepts of error control coding**(K4).**

UNIT-I

Analog Modulation – Need for modulation, AM, DSB-SC, SSB, VSB - Time domain and frequency domain description, single to NE modulation, power relations, Generation & Detection techniques, AM Transmitters, AM Receivers-Super-heterodyne receiver, IF,AGC.

UNIT-II

Angle Modulation: Phase and Frequency Modulation, Narrow band and Wideband FM, Carson's rule, Indirect and direct method of FM generation, Detection of FM, Phase locked loop, Comparison of FM and AM, FM Transmitters, FM Super-heterodyne receiver.

UNIT-III

Noise in Analog Communication system: Noise in DSB &SSB system, Noise in AM system, Noise in Angle Modulation system, Pre-emphasis and de-emphasis.

Pulse Modulation: Time Division Multiplexing, PAM, PWM, PPM-Generation and Detection.

UNIT-IV

DigitalModulationSystems: PulseModulation:Basebandsignals.Samplingprocess;QuantizationProcess;QuantizationNoise;Pulse-CodeModulation;NoiseConsiderationsinPCMSystems; Differential Pulse-Code Modulation, Delta modulation, adaptive delta modulation, Amplitude, phase and frequency shift keying schemes(ASK,PSK,FSK),introduction to M-array modulation schemes, Matched filter receivers and optimum receiver

UNIT-V

Information theory and Error control Coding: Measure of information, Entropy, Information rate, Source coding theorem, Channelcapacity–Shannon-Hartleylaw,controlCodes–Linearcodes,Cycliccodes,ConvolutionCoding-encoder, decoder-Exhaustive search and sequential method.

TEXTBOOKS:

1. SimonHaykinandMichaelMoher,"AnIntroductiontoAnalog&DigitalCommunications",2nd Ed.,Wiley,(2007).
2. H Taub& D. Schilling, Gautam Sahe, "Principles of CommunicationSystems",TMH,3rd Edition,(2007).
3. Tomasi,Wayne,"ElectronicsCommunicationSystems-Fundamentalsthroughadvanced",5thEdition,PearsonEducation,2009
4. Lathi,"ModernDigital&AnalogCommunicationsSystems",2e,OxfordUniversity Press
5. R. P. Singh, S. Sapre, "Communication Systems: Analog and Digital", Tata McGraw-Hill,2nd edition.

REFERENCEBOOKS:

1. BruceCarlson,Paul B.Crillyand Janet C.Rutledge, "CommunicationSystems:AnIntroductiontoSignalsandNoiseinElectrical Communications",4th Edition,McGraw-Hill,(2002).
2. SimonHaykin,"CommunicationSystems",4th Edition,John Wiley&Sons,(2001)
3. NevioBenvenuto, Roberto Corvaja, TomasoErseghe, and Nicola Laurenti,"CommunicationSystems:FundamentalsandDesignMethods",John Wiley&Sons,(2006).
4. SamShanmugam,K,"DigitalandAnalogCommunicationSystems",Wileypublisher(2006).

IV Sem.	Digital IC Applications	Course Code:V20ECT08	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of this course, the students Will be able to:

- CO1: Explain the structure of commercially available digital integrated circuit families. **[K2]**
- CO2:Learn the IEEE Standard 1076 Hardware Description Language (VHDL).**[K2]**
- CO3: Model complex digital systems at several levels of abstractions, behavioural, Structural, simulation, synthesis and rapid system prototyping.**[K2]**
- CO4: Analyze and design basic digital circuits with combinatorial and sequential logic Circuits using VHDL.**[K2]**
- CO5:Develop Programmable logic devices and memories with relevant ICs.**[K2]**

UNIT-I

Digital Logic Families and Interfacing: Introduction to logic families, CMOS logic, CMOS steady state and dynamic electrical behavior, CMOS logic families. Bipolar logic, transistor-transistor logic, TTL families, CMOS/TTL interfacing, Emitter coupled logic.

UNIT-II

Introduction to VHDL: Design flow, program structure, levels of abstraction, Elements of VHDL: Data types, data objects, operators and identifiers. Packages, Libraries and Bindings, Subprograms. VHDL Programming using structural and data flow modeling.

Behavioral Modeling: Process statement, variable assignment statement, signal assignment statement, wait statement , if statement, case statement ,null statement, loop statement, exit statement, next statement ,assertion statement, Inertial Delay Model, Transport Delay Model, Logic Simulation, Logic Synthesis, Inside a logic Synthesizer.

UNIT-III

Combinational Logic Design: Half adder, Full Adder, Ripple Adder, Binary Adder-Subtractor, Look Ahead Carry Generator, ALU, Decoders, encoders, multiplexers and DE multiplexers, parity circuits, comparators, Barrel Shifter, Simple Floating Point Encoder, Dual Priority Encoder, Design considerations of the above combinational logic circuits with relevant Digital ICs, modeling of above ICs using VHDL.

UNIT-IV

Sequential Logic Design: SSI Latches and flip flops, Shift Registers, Universal Shift Registers, Ring Counter, Johnson Counter, Ripple Counter, Design of Modulus N Synchronous Counters, Design considerations of the above sequential logic circuits with relevant Digital ICs, modelling of above ICs using VHDL.

UNIT-V

Memories:
ROM: Internal structure, 2D-Decoding, Commercial ROM types, timing and applications. Static RAM: Internal structure, SRAM timing, standard synchronous SRAMS. Dynamic RAM: Internal structure, timing, synchronous DRAMs.

Text Books:

1. Digital Design Principles & Practices – John F. Wakerly, PHI/ PearsonEducation Asia, 3rd Ed., 2005.

2. VHDL Primer – J. Bhasker, Pearson Education/ PHI, 3rd Edition.

References:

1. Fundamentals of Digital Logic with VHDL Design- Stephen Brown, ZvonkoVranesic, McGrawHill, 3rd Edition.

IV Sem.	Electro Magnetic Waves & Transmission Lines	Course Code:V20ECT09	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes: After Successful completion of this course, the students Will be able to:

- CO1:Find static electric field intensity by using various laws of electrostatics. **[K3]**
- CO2:Find static magnetic field intensity by using various laws of magneto statics and Develop the Maxwell's equations for time varying fields**. [K3]**
- CO3:Calculate the Propagation Characteristics of the EM Waves in different mediums And find Brewster angle, critical angle and total internal reflection**. [K3]**
- CO4:Compute Primary and Secondary constants for a given transmission line. **[K3]**
- CO5:Calculate reflection coefficient, VSWR etc. using smith chart. **[K3]**

Prerequisites: Review of Co-ordinate Systems.

UNIT-I: Electrostatics:

Coulomb's Law, Electric Field Intensity, Electric Flux Density, Gauss Law and Applications, Electric Potential, Relation between E and V, Energy Density, Convection and Conduction Currents, Dielectric Constant, Poisson's and Laplace's Equations; Capacitance – Parallel Plate, Coaxial Capacitors, Illustrative Problems.

UNIT-II: Magneto Statics:

Biot-Savart Law, Ampere's Circuital Law and Applications, Magnetic FluxDensity, Magnetic Scalar and Vector Potentials, Forces due to Magnetic Fields, Inductances and MagneticEnergy. Illustrative Problems**.**

Maxwell's Equations (Time Varying Fields):

Faraday's Law and Transformer EMF, Inconsistency of Ampere's Law and Displacement Current Density, Maxwell's Equations in Different Final Forms and Word Statements. Conditions at a Boundary Surface.

UNIT-III: EM Wave Characteristics:

Wave Equations for Conducting and Perfect Dielectric Media, Uniform Plane Waves – Definition, Relation Between E & H, Sinusoidal Variations, Wave Propagation in Lossy dielectrics, lossless dielectrics, free space, wave propagation in good conductors, Good Dielectrics, skin depth, Polarization & Types, Illustrative Problems.

Reflection and Refraction of Plane Waves – Normal and Oblique Incidences for Perfect Dielectrics, Brewster Angle, Critical Angle and Total Internal Reflection, Surface Impedance. Poynting Vector and Poynting Theorem. Illustrative Problems.

UNIT-IV: Transmission Lines - I:

Types, Applications of Transmission Lines, Equivalent Circuit, Primary & Secondary Constants, Transmission Line Equations for Finite and Infinite Lines, Characteristic Impedance, Propagation Constant, Phase and Group Velocities, , Lossless lines, Distortion less Lines, Illustrative Problems.

UNIT-V: Transmission Lines – II:

Input Impedance Relations, SC and OC Lines, Reflection Coefficient, VSWR. UHF Lines as Circuit Elements; λ/8, λ/4 and λ /2 Lines, Smith Chart – Construction and Applications, Single Stub Matching, Illustrative Problems.

TEXT BOOKS:

1. Elements of Electromagnetic – Matthew N.O. Sadiku, Oxford Univ. Press, 3rd ed., 2001.
2. Electromagnetic Waves and Radiating Systems – E.C. Jordan and K.G. Balmain, PHI, 2nd Edition, 2000.
3. Transmission Lines and Networks – UmeshSinha, SatyaPrakashan (Tech. India Publications), New Delhi, 2001.

REFERENCES:

1. Electromagnetic Fields and Wave Theory –GSN Raju, Pearson Education 2006
2. Engineering Electromagnetics – William H. Hayt Jr. and John A. Buck, TMH, 7th ed., 2006.
3. Electromagnetic Waves andTransmission Lines by Y. Mallikarjuna Reddy, Universities Press

V20MBT51: MANAGEMENT ECONOMICS & FINANCIAL ANALYSIS

(Effective for the students admitted into first year from the Academic Year 2020-2021)
(Common to all Engineering Branches under V20 Regulations)

L	T	P	C
3	0	0	3

COURSE OUTCOMES:

CO1: Understand the basic concepts of managerial economics, demand, elasticity of demand and methods of demand forecasting. (K2)

CO2: Interpret production concept, least cost combinations and various costs concepts in decision making. (K3)

CO3: Differentiate various Markets and Pricing methods along with Business Cycles (K2)

CO4: Prepare financial statements and its analysis. (K3)

CO5: Assess various investment project proposals with the help of Capital Budgeting techniques for decision making. (K3)

Unit-I

Introduction to Managerial Economics and demand Analysis: Definition of Managerial Economics and Scope-Managerial Economics and its relation with other subjects-Concept of Demand-Types-Determinants-Law of Demand its Exceptions-Elasticity of Demand-Types and Measurement-Demand forecasting and its Measuring Methods.

Unit-II

Production and Cost Analysis: Production function-Iso-quants and Iso-cost-Law of Variable proportions- Cobb-Douglas Production function-Economies of Scale-Cost Concepts- Opportunity Cost-Fixed vs Variable Costs-Explicit Costs vs Implicit Costs- Cost Volume Profit analysis-Determination of Break-Even Point- BEP Chart (Simple Problems).

Unit-III

Introduction To Markets, Pricing Policies & forms of Organizations and Business Cycles: Market Structures: Perfect Competition, Monopoly, Monopolistic and Oligopoly – Features – Price, Out-put Determination – Methods of Pricing: Evolution of Business Forms - Features of Sole Trader – Partnership – Joint Stock Company – State/Public Enterprises. Business Cycles – Meaning and Features – Phases of Business Cycle.

Unit-IV

Introduction to Accounting & Financing Analysis: Introduction to Double Entry System – Preparation of Financial Statements- Trading Account, Profit & Loss Account and Balance Sheet - Ratio Analysis – (Simple Problems).

Unit-V

Capital and Capital Budgeting: Capital Budgeting: Meaning of Capital-Capitalization-Meaning of Capital Budgeting-Need for Capital Budgeting-Techniques of Capital Budgeting-Traditional and Modern Methods.

TEXT BOOKS

1. Dr. N. AppaRao, Dr. P. Vijay Kumar: 'Managerial Economics and Financial Analysis', Cengage Publications, New Delhi – 2011
2. Dr. A. R. Aryasri – Managerial Economics and Financial Analysis, TMH 2011
3. Prof. J.V.Prabhakararao, Prof. P. Venkatarao. 'Managerial Economics and Financial Analysis', Ravindra Publication.

REFERENCES:

1. Dr. B. Kuberudu and Dr. T. V. Ramana: Managerial Economics & Financial Analysis, Himalaya Publishing House, 2014.
2. V. Maheswari: Managerial Economics, Sultan Chand.2014
3. Suma Damodaran: Managerial Economics, Oxford 2011.
4. VanithaAgarwal: Managerial Economics, Pearson Publications 2011.
5. Sanjay Dhameja: Financial Accounting for Managers, Pearson
. 6. Maheswari: Financial Accounting, Vikas Publications.
7. S. A. Siddiqui& A. S. Siddiqui: Managerial Economics and Financial Analysis, New Age International Publishers, 2012
8. Ramesh Singh, Indian Economy, 7th Edn., TMH2015
9. Pankaj Tandon A Text Book of Microeconomic Theory, Sage Publishers, 2015
10. Shailaja Gajjala and Usha Munipalle, Univerties press, 201

IV Sem.	Analog & Digital Communication Lab	Course Code: V20ECL04	L	T	P	C
			0	0	3	1.5

Syllabus Details

Course Outcomes: After Successful completion of this course, the students Will be able to:

CO-1- Demonstrate the operation of various pulse modulation and demodulation Techniques.**[K3]**
CO-2 -Construct the pre-emphasis and de-emphasis circuits and verify its frequency Response.**[K3]**
CO-3 -Demonstrate the spectrum analysis of modulated signal using spectrum analyser, Operation of AGC and PLL **[K3]**
CO-4- Distinguish the Time division multiplexing and DE multiplexing, Pulse digital Modulation Techniques **[K2]**
CO-5- Distinguish generation and detection of digital modulation techniques **[K2]**
CO-6- Verify the Source encoding and decoding (Huffman Coding) technique and channel Encoding and decoding techniques. **[K3]**

List of Experiments (Twelve experiments to be done)

A. Analog Communications

1. Amplitude Modulation - Mod. &Demod.
2. AM - DSB SC - Mod. &Demod.
3. Spectrum Analysis of Modulated signal using Spectrum Analyser
4. Pre-emphasis & De-emphasis
5. Frequency Modulation - Mod. &Demod, PLL.
6. Sampling Theorem - Pulse Amplitude Modulation - Mod. &Demod.
7. PWM, PPM - Mod. &Demod.

B. Digital Communications

1. Pulse code modulation, Differential pulse code modulation.
2. Delta modulation, Companding.
3. ASK, FSK, PSK.
4. Differential phase shift keying.
5. Source Encoder and Decoder
6. Channel coding-
    i. Linear Block Code-Encoder and Decoder
    ii. Binary Cyclic Code – Encoder and Decoder
    iii. Convolution Code – Encoder and Decoder

IV Sem.	Digital IC Application Lab	Course Code: V20ECL05	L	T	P	C
			0	0	3	1.5

Syllabus Details

Course Outcomes: After Successful completion of this course, the students Will be able to:

CO1: Identify the importance of various tools available in XILINX ISE12.2.**[K2]**
CO2: Develop VHDL/Verilog HDL Source code and perform simulation for various Combinational logic circuits using XILINX ISE12.2.**[K3]**
CO3: Develop VHDL/Verilog HDL Source code and perform simulation for various Sequential logic circuits using XILINX ISE12.2.**[K3]**

Note: The students are required to design and draw the internal logical structure of the following Digital Integrated Circuits and to develop VHDL/Verilog HDL Source code, perform simulation using relevant simulator and analyse the obtained simulation results using necessary synthesizer.

All the experiments are required to verify and implement the logical operations on the latest FPGA Hardware in the Laboratory.

List of Experiments:

(Minimum of Ten Experiments has to be performed)

1. Realization of Logic Gates
2. Design of Full Adder
3. Design of 3 to 8 Decoder –IC 74138
4. Design of 8 to 3 Encoder (with and without priority)
5. Design of 8 x 1 Multiplexer-IC 74151 and Dual 1x 4 De-multiplexer-IC 74155
6. Design of 4-Bit comparator-IC 7485
7. Design of D-Flip-Flop-IC 7474
8. Design of 4-Bit Ripple Counter.
9. Design of Decade counter –IC 7490
10. Design of Universal Shift register.
11. Design of RAM
12. Design of ALU.

Equipment/Software required:

1. Xilinx Vivado software / Equivalent Industry Standard Software
2. Xilinx Hardware / Equivalent hardware
3. Personal computer system with necessary software to run the programsand Implement.

Annexure-04

V20 Regulation

Semester III (Second Year)

Approved List of Courses offered to EEE Department by ECE Dept.

Sl. No.		Course Code	Course Title	Hours per Week			Credits
1.	Professional Core Course	V20ECT06	Analog Electronics	3	0	0	3
2.	Professional Core Course lab	V20ECL03	Analog Electronics lab	0	0	3	1.5

III Sem.	Analog Electronics	Course Code:V20ECT06	L	T	P	C
			3	0	0	3

Syllabus

Course Outcomes:
After Successful completion of the Course, the student will be able to:

CO-1: Explain the working principle of diode and Diode rectifier circuits with and without Filters.**(K2)**

CO-2: Sketch V-I characteristics of BJT and FET in different configurations (**K3)**

CO-3: Construct wave shaping circuits for various applications **(K3)**

CO-4: Construct circuits for different applications using ICs **(K3)**

CO-5: Explain the operation of Data Converters using IC 741 OP-AMP **(K2)**

UNIT-I Junction Diode Characteristics: p-n junction diode, current components in PN junction Diode, diode current equation, V-I Characteristics, Diode resistances, Breakdown mechanisms, Zener Diode.
Rectifiers: Basic Rectifier setup**,** half wave rectifier, full wave rectifier, bridge rectifier, derivations of characteristics of rectifiers, Filters- Inductor filter, Capacitor filter, derivation for ripple factor in each case, Zener diode as Voltage Regulator.

UNIT-II Transistor Characteristics: BJT: Junction transistor, transistor current components, transistor equation, transistor configurations and characteristics of transistor in Common Base, Common Emitter and Common Collector configurations, punch through/ reach through, transistor as an amplifier.
FET: FET types, construction, operation, characteristics, parameters, MOSFET-types, construction, operation, characteristics, comparison between JFET and MOSFET.

UNIT-III Wave shaping circuits: Response of high pass and low pass RC circuits to step, pulse, Square inputs. High pass RC circuit as differentiator, low pass RC circuit as integrator. Series and shunt clippers, clipping at two independent levels, Positive and Negative Clampers.

UNIT-IV Integrated Circuits and applications: Op-amp Block Diagram, Ideal Op-amp, Equivalent Circuit, Ideal voltage transfer curve, open loop op-amp configurations. Inverting and non-inverting amplifiers, summing, scaling, averaging amplifier, integrator and differentiator, 555 timer functional block diagram, A stable and Monostable multivibrators.

UNIT-V Data Converters: Weighted resistor DAC, R-2R ladder DAC. Flash Type ADC; counter type ADC, Successive approximation ADC, Dual slope ADC, Specifications of DAC&ADC.

TEXT BOOKS:

1. Integrated Electronics- J. Millman and C.C. Halkias, TMH
2. Electronic Devices and Circuits- Salivahanan, N.Suresh Kumar, A. Vallavaraj, TMH
3. Pulse, Digital and Switching Waveforms - J. Millman and H. Taub, TMH
4. Linear Integrated Circuits – D. Roy Choudhury, 4th edition, New Age International (p) Ltd.
5. Op-Amps & Linear Integrated Circuits - Ramakanth A. Gayakwad,3rd edition, PHI.

REFERENCE BOOKS:

1. Electronic Devices and Circuits Theory – Robert L. Boylestad and Louis Nashelsky, Pearson/Prentice Hall.
3. Pulse & Digital Circuits-BN Yoga Narasimhan, 2000,SriMaruthi Publishers, Bangalore.
4. Operational Amplifiers & Linear Integrated Circuits –Sanjay Sharma; SKKataria& Sons;2nd Edition,2010

III Sem.	Analog Electronics Lab	Course Code: V20ECL03	L	T	P	C
			0	0	3	1.5

Course Outcomes: After Successful completion of the Course, the student will be able to:

CO-1:Interpret the Characteristics of various semiconductor devices. **(K2)**

CO-2: Examine the Performance of Rectifiers with and without Filters. **(K3)**

CO-3: Construct circuit for linear wave shaping circuits. **(K3)**

CO-4: Construct circuits for verifying linear and nonlinear applications using IC741op-amp And IC 555 timer **(K3)**

CO-5:Verify the Characteristics of 4 bit Digital to Analog Converter **(K3)**

List of Experiments: (Any 10 Experiments to be done)

1. PN Junction diode characteristics
2. Rectifiers with and without filters
   Part A: Half Wave Rectifier, Part B: Full Wave Rectifier
3. Zener diode Characteristics
   Part A: V-I characteristics, Part B: Zener diode as Voltage Regulator
4. BJT Characteristics (CE Configuration)
   Part A: Input characteristics, Part B: Input characteristics
5. JFET Characteristics (CS Configuration)
   Part A: Drain characteristics, Part B: Transfer characteristics
6. Linear Wave Shaping
   Part A: High Pass RC Circuit, Part B: Low Pass RC Circuit
7. Non-linear Wave Shaping - Clippers
   Part A: Unbiased Clippers, Part B: Biased Clippers
8. Non-linear Wave Shaping - Clampers
   Part A: Unbiased Clampers, Part B: Biased Clampers
9. Summing, Scaling, Averaging amplifiers using IC 741.
10. Differentiator and Integrator Circuits using IC 741.
11. A stable Multi vibrator using IC 555
12. . 4 bit Digital to Analog to Digital Converter

Approved Course structure for B. Tech ECT (V20)

COURSE STRUCTURE

(For V20 Regulation)

ECT

V20 Regulation

Semester III (Second Year)

Sl. No.	Course Category	Course Code	Course Title	Hours per Week			Credits
1.	Basic Science Courses		Mathematics-III **(M-III)**	3	0	0	3
2.	Professional Core Course	V20ECT02	Electronic Devices, Circuits & Analysis **(EDCA)**	3	0	0	3
3.	Professional Core Courses		Probability Theory Stochastic Process **(PTSP)**	3	0	0	3
4.	Professional Core Courses	V20ECT04	Network Theory **(NT)**	3	0	0	3
5.	Professional Core Courses	V20ECT05	Signals & Systems **(SS)**	3	0	0	3
6.	Professional Core Courses (LAB)	V20ECL01	Electronic Devices, Circuits & Analysis Lab **(EDCA LAB)**	0	0	3	1.5
7.	Professional Core Courses (LAB)	V20ECL02	Signals & Systems Lab **(SS LAB)**	0	0	3	1.5
8.	Professional Core Courses (LAB)	V20CSL31	Data Structures Lab **(DS LAB)**	0	0	3	1.5
9	**Skill Oriented Course***	V20ECSOC01	Certificate course being offered by industries/ professional bodies/ APSSDC or any other accredited bodies	**1**	**0**	**2**	**2**
10	Mandatory Course (AICTE suggested)	V20ENT02	Professional Communication Skills **(PCS-I)**	2	0	0	0
						Total Credits	**21.5**

Semester IV (Second Year)

Sl. No.	Course Category	Course Code	Course Title	Hours			Credits
				L	**T**	**P**	
1.	EngineeringScience Courses	V20EET11	Control Systems **(CS)**	3	0	0	3
2.	Basic Science Course/Prof Core Course	V20ECT07	Analog & Digital Communication **(ADC)**	3	0	0	3
3.	Professional Core Courses	V20ECT08	Digital IC Applications **(DICA)**	3	0	0	3
4.	Professional Core Courses	V20ECT09	Electro Magnetic Waves & Transmission Lines **(EMTL)**	3	0	0	3
5.	Humanities and Social Sciences	V20MBT51	Managerial Economics & Financial Analysis (**MEFA)**	3	0	0	3
6.	EngineeringScience Courses/Prof Core (Interdisciplinary) (LAB)	V20CSL33	Python Programming Lab	0	0	3	1.5
7.	Professional Core Courses (LAB)	V20ECL04	Analog & Digital Communication Lab **(ADC LAB)**	0	0	3	1.5
8.	Professional Core Courses (LAB)	V20ECL05	Digital IC Applications Lab **(DICA LAB)**	0	0	3	1.5
9	**Skill Oriented Course***	V20ECSOC02	Certificate course being offered by industries/ professional bodies/ APSSDC or any other accredited bodies	**1**	**0**	**2**	**2**
10	Mandatory Course (AICTE suggested)	V20ENT03	Professional Communication Skills **(PCS-II)**	2	0	0	0
						Total Credits	**21.5**

	Internship 2 Months (Mandatory) during Summer vacation				
	Honors/Minor Courses (The Hours Distribution can be 3-0-2 or 3-1-0 also)	**4**	0	**0**	**4**

***Skill Oriented Course:**

The Student shall be given an option to choose either the skill courses being offered by the college or to choose a certificate course being offered by industries/ professional bodies/ APSSDC or any other accredited bodies as approved by the concerned BoS.

List of Skill Oriented Courses:

S. No	Name of the Proposed Course
1	PCB Design
2	Programming in Scilab
3	Programming with Arduino
4	Circuit Design & Simulation using Multisim
5	Concepts of Embedded systems
6	Internet of Things
7	Robotics
8	Hands on Graphical Programming Using Labview

Approved Course structure & Syllabus for M. Tech (V21)

COURSE STRUCTURE
AND
DETAILED SYLLABUS

For

M. Tech

(Embedded Systems & VLSI)

Academic Year 2021-2022

ELECTRONICS & COMMUNICATION ENGINEERING

BRANCH

SRI VASAVI ENGINEERING COLLEGE
(AUTONOMOUS)

(Sponsored by Sri Vasavi Educational Society)
Approved by AICTE, New Delhi and Permanently Affiliated to JNTUK, Kakinada
Pedatadepalli, **TADEPALLIGUDEM – 534 101,** W.G. Dist., (A.P.)

COURSE STRUCTURE

Course Structure for
M. Tech (Embedded Systems &VLSI) w.e.f A.Y 2021-22

I Semester

Sl. No.	Course Code	Course Name	L	T	P	C
1.	V21ESVT01	System Design through VERILOG	3	-	-	3
2.	V21ESVT02	Embedded Systems Design	3	-	-	3
3.	V21ESVT03 V21ESVT04 V21ESVT05	**ELECTIVE-1** Programming Languages for Embedded Systems Parallel processing System On Chip & Applications	3	-	-	3
4.	V21ESVT06 V21ESVT07 V21ESVT08	**ELECTIVE-II** Digital System Design CPLD & FPGA Architectures And Applications VLSI Signal Processing	3	-	-	3
5.		Research methodology and IPR	2	0	0	2
6.	V21ESVL01	System Design through Verilog Lab	-	-	4	2
7.	V21ESVL02	Embedded Systems Design Lab		-	4	2
8.	Aud. 1	Audit Course 1	2	0	0	0
			16	**0**	**8**	**18**

Total Contact Hours: 24 **Total Credits: 18**

II Semester

Sl. No.	Course Code	Course Name	L	T	P	C
1.	V21ESVT09	Analog and Digital CMOS VLSI Design	3	-	-	3
2.	V21ESVT10	Real Time Operating Systems	3	-	-	3
3.	V21ESVT11 V21ESVT12 V21ESVT13	**ELECTIVE-III** MEMS Technology & Applications Design for Testability Semiconductor Memory Design And Testing	3	-	-	3
4.	V21ESVT14 V21ESVT15 V21ESVT16	**ELECTIVE-IV** Hardware Software Co-Design Embedded Computing Communication Buses and Interfaces	3	-	-	3
5.	V21ESVL03	Analog and Digital CMOS VLSI Design Lab	-	-	4	2
6.	V21ESVL04	Real time Operating Systems Lab		-	4	2
7.	V21ESVL05	Mini project	0	0	4	2
8.	Aud. 2	Audit course 2	2	0	0	MNC
			14	**0**	**12**	**18**

Total Contact Hours: 26 **Total Credits: 18**

III Semester*

Sl. No.	Course Code	Course Name	L	T	P	Credits
1.	V21ESVT17 V21ESVT18 V21ESVT19	1.IOT and its Applications 2.Low Power VLSI Design 3.MOOCs Course	3	0	0	3
2.	V21ESVOE01	1.Operations Research 2.Cost Management of Engineering projects 3. MOOCs Course	3	0	0	3
3.	V21ESVP01	Dissertation phase-I/Industrial Project **(to be continued and evaluated next semester)**	0	0	20	10#
					Total Credits	**16**

Evaluated and Displayed in IV semester Marks list**.**

*Students going for Industrial project/Thesis will complete these courses through MOOCs

IV Semester

Sl. No.	Course Code	Course Name	P.Os	Category	L	T	P	C
1.	V21ESVP02	Project/Dissertation phase-II (continued from III semester)			0	0	32	16
							Total Credits	**16**

Total Credits : 66

Audit course 1&2

1. English for Research paper Writing

2. Disaster Management

3. Value Education

4. Constitution of India

5. Pedagogy Studies

6. Stress Management by Yoga

7. Personality Development through Life Enlightenment Skills

I Semester

SYLLABUS

I Sem.	SYSTEM DESIGN THROUGH VERILOG	Course Code: V21ESVT01	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes:

- CO1: Outline basic concepts of RTL code for digital circuits **[K2]**
- CO2: Model RTL codes for digital circuit at gate and data flow level **[K3]**
- CO3: Model RTL codes for digital circuit at behavioural level **[K3]**
- CO4: Model RTL codes for digital circuit at switch level modelling and outline the concepts of task, function and complier directives **[K3]**
- CO5: Analyze Synthesize of Combinational and Sequential Circuits **[K4]**

UNIT-I
INTRODUCTIONTOVERILOG:
Verilog as HDL, Levels of design description, concurrency, module, simulation and synthesis, testbench, functional verification,programminglanguageinterface (PLI),simulationand synthesistools.

LANGUAGECONSTRUCTSANDCONVENTIONS:
Introduction, keywords, identifiers, whitespace characters, comments, numbers, strings, logic values, data types, scalars and vectors, parameters, memory, operators,systemtasks.

UNIT-II
GATELEVELMODELLING:
Introduction,AND gate primitive, module structure, other gate primitives, illustrative examples, tristate gates, arrayof instances of primitives, design of Flip flops with gate primitives, delays, strengths and contention resolution, nettypes,designofbasic circuits.

DATA FLOWLEVEL MODELLING
Introduction, continuous assignment structures, delays and continuous assignments, assignment to vectors.

UNIT-III
BEHAVIORALMODELLING:
Introduction, operationsandassignments,initial construct,alwaysconstruct,examples,assignmentswith delays, wait construct, multiple always blocks, designs at behavioral level, blocking and non-blocking assignments, the case statement, if and if else constructs, assign-De assign construct,repeat construct, FOR loop, the disable construct, While loop, Forever loop, parallel blocks, force-release construct,event.

UNIT-IV
SWITCHLEVELMODELLING
Basictransistor switches, CMOS switch, Bidirectional gates and time delays with switch primitives, instantiations withstrengthsanddelays,strengthcontentionwithtriregnets, switch level modeling for NAND, NOR and XOR.

SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES: Introduction, System Tasks and Functions, File based Tasks and Functions, Compiler Directives, Hierarchical Directives, User-defined Primitives (UDP), FSM Design (Moore and Melay Machines).

UNIT-V

SYNTHESISOFCOMBINATIONAL ANDSEQUENTIAL LOGIC USINGVERILOG: Synthesisof combinational logic: Net list of structured primitives, a set of continuous assignment statements and level sensitivecyclic behavior with examples, Synthesis of priority structures, Exploiting logic don't care conditions. Synthesis ofsequential logic with latches: Accidental synthesis of latches and Intentional synthesis of latches, Synthesis ofsequentiallogicwithflip-flops,Synthesisofexplicitstatemachines.

TEXTBOOKS:

1. DesignthroughVerilogHDL—T.R.PadmanabhanandB. BalaTripuraSundari,WSE, IEEEPress,2004.
2. AdvancedDigitalDesignwithVerilog HDL—MichaelD.Ciletti,PHI,2005.

REFERENCES:

1. FundamentalsofLogicDesignwithVerilog—Stephen.BrownandZvonkoVranesic,TMH,2005.
2. AVerilogPrimier—J.Bhasker,BSP,2003.

I Sem.	EMBEDDED SYSTEM DESIGN	Course Code: V21ESVT02	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome:

The student will be able to

- CO1: Illustrate the ARM architecture and its memory management.**(K2)**
- CO2: Describe the ARM instruction set for ARM programming.**(K2)**
- CO3: Describe Thumb instruction set for ARM programming.**(K2)**
- CO4: Explain the basics of ARM Cortex-M3**(K2)**
- CO5: Explain ARM Cortex-M3 interfacing.**(K2)**

UNIT-I:

ARM Architecture ARM Design Philosophy, Registers, PSR, Pipeline, Interrupts and Vector Table, Architecture Revision, ARM Processor Families. Introduction to ARM Cortex.

UNIT-II:

ARM Programming Model-I Instruction Set**:** Data Processing Instructions, Branch, Load, Store Instructions, PSR Instructions, Conditional Instructions.

UNIT-III:

ARM Programming Model-II Thumb Instruction Set**:** Register Usage, Other Branch Instructions, Data Processing Instructions, Single-Register and Multi Register Load-Store Instructions, Stack, Software Interrupt Instructions.

UNIT-IV

Introduction to ARM Cortex-M3 Processor**-**What Is the ARM Cortex-M3 Processor,Background of ARM and ARM Architecture,Instruction Set Development**,** The Thumb-2 Technology and Instruction Set Architecture**,** Cortex-M3 Processor Applications.

Cortex-M3 Basics-Registers, Operation Mode**,** Exceptions and Interrupts**,** Vector Tables**,** Stack Memory Operations, Reset Sequence

UNIT-V

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor call and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Interrupt Configuration.

Cortex-M3 Implementation Overview-the Pipeline, A detailed block diagram, Bus Interfaces on the Cortex-M3,Other Interfaces on the Cortex-M3, the External PPB, Typical Connections,Reset Types and Reset Signals.

TEXT BOOKS:

1. ARM Systems Developer's Guides- Designing & Optimizing System Software – Andrew N. Sloss, Dominic Symes, Chris Wright, 2008, Elsevier.
2.The Definitive Guide to the ARM® Cortex-M3 Second Edition-Joseph Yiu
3. ARM System-on-chip Architecture- Stephen Bo Furber - Addison-Wesley, 2000

REFERENCE BOOKS:

1. Embedded Microcomputer Systems, Real Time Interfacing – Jonathan W. Valvano – Brookes / Cole, 1999, Thomas Learning.

I Sem.	Programming Languages for Embedded Systems (Elective-I)	Course Code: V21ESVT03	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes:

At the end of this course, students will be able to

- CO1: Write an embedded C application of moderate complexity. **(K2)**
- CO2: Develop and Analyze algorithms in C++.**(K3)**
- CO3: Differentiate interpreted languages from compiled languages. **(K2)**
- CO4 : Describe the Overloading and Inheritance **(K2)**
- CO5: Differentiate the Function Template and Class Templates **(K2)**

UNIT-I: Embedded „C" Programming Bitwise operations, Dynamic memory allocation, OS services. Linked stack and queue, sparse matrices, Binary tree. Interrupt handling in C, Code optimization issues. Embedded Software Development Cycle and Methods (Waterfall, Agile)

UNIT-II: Object Oriented Programming Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism

UNIT-III: CPP Programming: „cin", „cout", formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, „this" pointer, constructors, destructors, friend function, dynamic memory allocation

UNIT-IV: Overloading and Inheritance: Need of operator overloading, overloading the assignment, Overloading using friends, type conversions, single inheritance, base and derived classes, friend Classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, Polymorphism, virtual functions.

UNIT-V: Templates: Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch-throw, Multiple Exceptions. Scripting Languages:

Overview of Scripting Languages – PERL, CGI, VB Script, Java Script.
PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied Variables, Inter process Communication Threads, Compilation & Line Interfacing.

Text Books:

1. Michael J. Pont, "Embedded C", Pearson Education, 2nd Edition, 2008
2. Randal L. Schwartz, "Learning Perl", O"Reilly Publications, 6th Edition 2011

Reference Books:

1. A. Michael Berman, "Data structures via C++", Oxford University Press, 2002
2. Robert Sedge wick, "Algorithms in C++", Addison Wesley Publishing Company, 1999
3. Abraham Silberschatz, Peter B, Greg Gagne, "Operating System Concepts", John Willey& Sons, 2005Kaufmann.

I Sem.	Parallel Processing (Elective I)	Course Code: V21ESVT04	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes:

At the end of this course, students will be able to

- CO1: Identify limitations of different architectures of computer **(K2)**
- CO2: Analysis quantitatively the performance parameters for different Architectures **(K2)**
- CO3: Investigate issues related to compilers and instruction set based on type of Architectures. **(K2)**
- CO 4: Describe the Multi threaded Architectures and Processors **(K2)**
- CO5: Explain the Parallel Programming Techniques **(K2)**

UNIT-I: Overview of Parallel Processing and Pipelining, Performance analysis, Scalability

UNIT-II: Principles and implementation of Pipelining, Classification of pipelining processors, Advanced pipelining techniques, Software pipelining

UNIT-III: VLIW processors Case study: Superscalar Architecture- Pentium, Intel Itanium Processor and Ultra SPARC,MIPS on FPGA, Vector and Array Processor, FFT Multiprocessor Architecture

UNIT-IV: Multithreaded Architecture, Multithreaded processors, Latency hiding techniques, Principles of multithreading, Issues and solutions

UNIT-V: Parallel Programming Techniques: Message passing program development, Synchronous and asynchronous message passing, Shared Memory Programming, Data Parallel Programming, Parallel Software Issues. Operating systems for multiprocessors systems customizing applications on parallel processing platforms

Text Books:

1. Kai Hwang, Faye A. Briggs, “Computer Architecture and Parallel Processing”, MGH International Edition
2. Kai Hwang, “Advanced Computer Architecture”, TMH
3. V. Rajaraman, L. Sivaram Murthy, “Parallel Computers”, PHI.

Reference Books:

1. William Stallings, “Computer Organization and Architecture, Designing for Performance“Prentice Hall, Sixth edition
2. Kai Hwang, ZhiweiXu, “Scalable Parallel Computing”, MGH
3. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, Morgan

I Sem.	System on Chip & Applications (Elective I)	Course Code: V21ESVT05	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome:

The student will be able to

- CO1: Describe SOC System Approach, design and its Architecture –**[K2]**
- CO2: Discuss the selection of processor and its micro architecture for SOC –**[K2]**
- CO3: Discuss Memory Design for SOC –**[K2]**
- CO4: Explain the concepts of bus models and Interconnect Architectures –**[K2]**
- CO5: Explain SOC based Applications –**[K2]**

UNIT-I

Introduction to the System Approach System Architecture, Components of the system,Hardware & Software, Processor Architectures, Memory and Addressing.System level interconnection, an approach for SOC Design, System Architecture and Complexity.

UNIT-II

Processors Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT-III

Memory Design for SOC Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT-IV

Interconnect Customization and Configuration Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT-V

Application / Case Studies:

Zynq system on chip design – Secure Boot, Analog Data Acquisition, System Monitoring using the Zynq-7000 AP SOC Processing System with the XADC AXI Interface.

Cypress- PSoC4- Architecture, GPIO Pins and its applications - down counter, sine wave Generator using PSOC 4 device.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.
3. Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC-Louise H. Crockett Ross A. Elliot Martin A. Enderwitz Robert W. Stewart
4. Cypress PSoC User Manual

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques – PrakashRashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

I Sem.	Digital System Design (Elective II)	Course Code: V21ESVT06	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome:

The student will be able to

- CO1: Describe the algorithms for minimization of functions **(K2)**
- CO2: Describe the algorithms for minimization of PLDs. **(K2)**
- CO3: Design large scale digital systems. **(K3)**
- CO4: Discuss the fault model and diagnosis in combinational Circuits. **(K2)**
- CO5**:** Discuss the fault model and diagnosis in sequential Circuits **(K2)**

UNIT-I: Minimization Procedures and CAMP Algorithm

Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs, CAMPI algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II: PLA Design, PLA Minimization and Folding Algorithms

Introduction to PLDs, basic configurations and advantages of PLDs, PLA-Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm (IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT -III: Design of Large Scale Digital Systems

Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design and PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT-IV: Fault Diagnosis in Combinational Circuits

Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V: Fault Diagnosis in Sequential Circuits

Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS:

1. Logic Design Theory-N. N. Biswas, PHI
2. Switching and Finite Automata Theory-Z. Kohavi, 2nd Edition, 2001, TMH
3. Digital system Design using PLDd-Lala

REFERENCE BOOKS:

1. Fundamentals of Logic Design – Charles H. Roth, 5th Ed., Cengage Learning.
2. Digital Systems Testing and Testable Design – MironAbramovici, Melvin A. Breuer and Arthur D. Friedman- John Wiley & Sons Inc.

I Sem.	CPLD & FPGA Architectures and Applications (Elective II)	Course Code: V21ESVT07	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome:

The student will be able to

- CO1: Describe the Programmable Logic Devices **(K2)**
- CO2: Distinguish the various types of Field Programmable Gate Arrays **(K2)**
- CO3: Apply the typical applications on FPGAs **(K3)**

UNIT-I: Introduction to Programmable Logic Devices

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices –Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT-II: Field Programmable Gate Arrays

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs and Applications of FPGAs.

UNIT –III: SRAM Programmable FPGAs:

Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT –IV: Anti-Fuse Programmed FPGAs

Introduction, Programming Technology, Device Architecture, the Actel ACT1, ACT2 and ACT3 Architectures.

UNIT –V: Design Applications

General Design Issues, Counter Examples, a Fast Video Controller, A Fast DMA Controller and Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

TEXT BOOKS:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.

2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.

2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/ SamihaMourad, Pearson Low Price Edition.

3. Digital Systems Design with FPGAs and CPLDs - Ian Grout, Elsevier, Newnes.

4. FPGA based System Design - Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

I Sem.	VLSI Signal Processing (Elective II)	Course Code:V21ESVT08	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes
On successful completion of the module, students will be able to:

CO1: Illustrate the existing or new DSP architectures suitable for VLSI**.(K2)**
CO2: Understand the concepts of folding and unfolding algorithms and applications **.(K2)**.
CO3: Implement fast convolution algorithms. **.(K2)**
CO4: Describe Low power design aspects of processors for signal processing and wireless Applications. **.(K2)**
CO5: Explain Low Power Design, Scaling Vs. Power Consumption, Power Analysis **.(K2)**

UNIT -I
Introduction to DSP: Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

UNIT –II
Folding and Unfolding: Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multi rate systems
Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT -III
Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT -IV
Fast Convolution: Introduction – Cook-Toom Algorithm – Winograd algorithm – Iterated Convolution –Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

Unit V: Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, lowpower design. Low Power Design: Scaling Vs. Power Consumption, Power Analysis, Power Reduction techniques,Power Estimation Approaches

Text Books:

1. Keshab K. Parthi[A1], VLSI Digital signal processing systems, design and Implementation [A2],Wiley, Inter Science, 1999.
2. Mohammad Isamail and Terri Fiez, Analog VLSI signal and information processing, McGrawHill, 1994
3. S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, Prentice Hall,1985.

I Sem.	System Design through Verilog Lab	Course Code: V21ESVL01	L	T	P	C
			0	0	4	2

Syllabus Details

COURSE OUTCOMES:

- CO1: Develop the simulation of combinational and sequential circuits using HDL Language.**[K3]**
- CO2: Develop the synthesis of combinational and sequential circuits using HDL Language.**[K3]**
- CO3: Analyze the implemented of digital logics with hardware module kit FPGA **[K4]**

The students are required to design the Verilog codes to perform the following experiments using necessary simulator (Xilinx ISE Simulator) to verify the logic functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer) and then verify the implemented logic function with hardware kits (FPGA kits).

The students are required to acquire the knowledge in the platform Xilinx by perform at least 10 experiments.

List of Experiments:

1) Logic gates
2) Adder-Subtractor
3) Multiplexer and DE multiplexer
4) Encoder and Decoder
5) ALU
6) Fire detection and control system using Combinational Logic Circuits
7) Flip Flops
8) LFSR
9) Up counter/Down counter
10) Synchronous RAM
11) Pattern detector using Moore/Melay machine
12) Traffic light controller using sequential logic circuit.
13) UART

I Sem.	Embedded Systems Design Lab	Course Code: V21ESVL02	L	T	P	C
			0	0	4	2

Syllabus Details

Course Outcomes:

At the end of the laboratory work, students will be able to:

- **CO1:** Develop applications based on ARM Cortex-M3 processor using Cortex-M3 Development boards on the platform of co-coox and Arduino IDE.-**K3**
- **CO2:** Develop the applications based on DSP C6713 evaluation kits and using Code Composer Studio (CCS).-**K3**

List of Assignments:

Part A:

Experiments to be carried out on Cortex-M3 development boards and using GNU Tool chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. Control intensity of an LED using PWM implemented in software and hardware.
3. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
4. UART Echo Test.
5. Take Analog readings on rotation of rotary potentiometer connected to an ADC channel.
6. Temperature indication on an RGB LED.
7. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
8. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
9. System reset using watchdog timer in case something goes wrong.
10. Sample sound using a microphone and display sound levels on LEDs.

Part B:

Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

1. To develop a C code to compute Euclidian distance between any two Points.
2. To develop a C code for implementation of convolution operation.
3. To develop a C code to compute FFT.
4. To design and implement filters in C to enhance the features of given input sequence/signal.

Lab Requirements:

1. Coo-coX Software PlatForm.
2. Arduino IDE
3. Code Composer Studio(CCS)

Hardware:

1. The Development kits of ARM-Cortex Boards
2. DSP C6713 evaluation kits
3. Sensors for Interfacing
4. Serial cables, Network Cables and Recommended power Supply for the board.

II Semester
SYLLABUS

II Sem.	Analog and Digital CMOS VLSI Design	Course Code: V21ESVT09	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes:

At the end of the laboratory work, students will be able to:

CO1: Describe the concept of MOS structure and physical design of CMOS **(K2)**

CO2: Design the CMOS Inverters and various CMOS combinational logic circuits **(K4)**

CO3: Design the CMOS different Sequential logic circuits **(K4)**

CO4: Describe the concept of modelling of MOS and Analog CMOS Sub-Circuits **(K2)**

CO5: Describe the CMOS Op-Amps & it's Applications. **(K2)**

UNIT-I: **Review of MOS structures and Physical design flow:**
Basic MOS structure and its static behaviour, Quality metrics of a digital design: Cost,Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models.Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic.

UNIT-II CMOS INVERTER AND COMBINATIONAL LOGIC:
Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and theirEvaluation, Dynamic behaviour, Power consumption. Combinational logic: Static CMOSdesign, Logic effort, Rationed logic, Pass transistor logic, Dynamic logic, Speed and powerdissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic.

UNIT-III SEQUENTIAL LOGIC:
Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops,Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining,Pulse registers, and Non-bistable sequential circuit.

UNIT -IV CMOS MODELING AND ANALOG SUB- CIRCUITS
CMOS Device Modelling - Simple MOS Large-Signal Model, Other Model Parameters,Small-Signal Model for the MOS Transistor, Sub-threshold MOS Model. MOS Switch, MOSDiode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Cascode currentMirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT-V CMOS AMPLIFIERS:
Inverters- Active load inverter, current source inverter, push-pull inverter, DifferentialAmplifiers- large signal analysis, small signal analysis, Cascode Amplifiers, CurrentAmplifiers, Output Amplifiers, Design of CMOS Op Amps, Compensation of Op Amps,Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two-Stage Op Amps,Cascode Op Amps, Characterization of Comparator, Two-Stage comparator design.

II Sem.	Real Time Operating Systems	Course Code: V21ESVT10	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes
Upon the completion of the course student will be able to

- CO1: Illustrate real time programming concepts. **(K2)**
- CO2: Apply RTOS functions to implement embedded applications **(K2)**
- CO3: Understand fundamentals of design consideration for embedded
- Applications. **(K2)**
- CO4: Describe the Concepts of Exceptions and Interrupts **(K2)**
- CO 5: Explain the Concepts of Synchronization and Communication **(K2)**

UNIT-I
Introduction to Real-Time Operating Systems - Defining an RTOS, The scheduler, Kernel Objects and services, Key characteristics of an RTOS
Task- Defining a Task, Task States and Scheduling, Typical Task Operations, Typical Task Structure, Synchronization, Communication and Concurrency

UNIT-II
Semaphores - Defining Semaphores, Typical Semaphore Operations, Typical Semaphore Use
Message Queues - Defining Message Queues, Message Queue States, Message Queue Content, Message Queue Storage, Typical Message Queue Operations, Typical Message Queue Use, Pipes, Event Registers, Signals and condition Variables

UNIT-III
Exceptions and Interrupts - Exceptions and Interrupts, Applications of Exceptions and Interrupts, Closer look at exceptions and interrupts, processing general Exceptions, Nature of Spurious Interrupts
Timer and Timer Services - Real-Time clocks and System Clocks, Programmable Interval Timers, Timer Interrupt Service Routines.
I/O Subsystems - I/O concepts, I/O subsystems

UNIT-IV
Memory Management - Dynamic Memory Allocation in Embedded Systems, Fixed-Size Memory management in Embedded Systems, Blocking VS. Non-Blocking Memory Functions, Hardware Memory Management Units
Modularizing an application for concurrency- An outside-in approach to decompose Applications, Guidelines and Recommendations for Identifying Concurrency, Scheduleability Analysis

UNIT-V
Synchronization and Communication - Synchronization, Communication, Resource Synchronization Methods, Critical section, Common practical design patterns, Specific Solution Design Patterns,
Common Design Problems - Resource Classification, Deadlocks, Priority Inversion.

Text Books

1. Qing Li, Caroline Yao (2003), “Real-Time Concepts for Embedded Systems”, CMP Books.

Reference Books

1. Albert Cheng, (2002), “Real-Time Systems: Scheduling, Analysis and Verification”, WileyInterscience.

2. Hermann Kopetz, (1997), “Real-Time Systems: Design Principles for Distributed EmbeddedApplications”, Kluwer.

3. Insup Lee, Joseph Leung, and Sang Son, (2008) “Handbook of Real-Time Systems”, Chapman andHall.Krishna and Kang G Shin, (2001), “Real-Time Systems”, McGraw Hill.

II Sem.	MEMS Technology and its Applications (Elective-III)	Course Code: V21ESVT11	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome:
The student will be able to

- CO1: Describe the concepts of MEMS and Microsystems. **(K2)**
- CO2: Describe various possible materials for MEMS based devices. **(K2)**
- CO3: Describe various process steps involved in fabrication of MEMS devices. **(K2)**
- CO4: Describe various micro sensors and micro actuators. **(K2)**
- CO5: Describe various MEMS devices and their applications. **(K2)**

UNIT-I:

MEMS AND MICROSYSTEM
Introduction to MEMS, Microsystems and microelectronics, Multidisciplinary nature of MEMS, Miniaturization and its Benefits, Scaling laws in Miniaturization, MEMS Design Considerations, Advantages of MEMS Technology, Applications of MEMS

UNIT-II:

MATERIALS FOR MEMS
Introduction, Substrates & wafers, Active Substrate Materials, Silicon as a Substrate Material, Silicon Compounds, Piezoelectric Crystals, Polymers, Packaging Materials.

UNIT-III:

MICROFABRICATION
Introduction, Fabrication Process – Wafer processing, Photolithography, Ion implantation, Oxidation, Chemical vapor deposition (CVD), Physical vapor deposition, Deposition by Epitaxy, Etching, Manufacturing Process -Bulk Micromachining, Surface Micromachining and LIGA Process, Packaging technology, System level packaging, single and multichip packaging. Microsystem packaging, interfacingsin Microsystem packaging.

UNIT-IV:

MEMS BASED SENSORS AND ACTUATORS
Introduction, working principles of Microsystem - Micro Sensors, Micro Actuators and MEMS with Micro sensors: Pressure sensors, Temperature sensors, Humidity sensors, Accelerometers, Gyroscopes, Biomedical Sensors, Chemical sensors, MEMS with micro actuators: Microgrippers, Micromotors, Micro gears and Micropumps. Microfluidics.

UNIT-V:
RF MEMS
RF MEMS devices: Switch parameters- Basics of switching - Mechanical Switches-Electronic switches for RF and microwave applications – Approaches for low-actuation-voltage switches, MEMS based Reconfigurable Antennas, Reconfigurable Filters and Phase shifters.

Textbooks:

1. Tai-Ran Hsu, MEMS and Microsystems: Design, Manufacture, and Nanoscale Engineering, 2nd Edition, John Wiley & Sons, Inc., Hoboken, New Jersey, 2008.
2. Gabriel M Rebeiz, "RF MEMS - Theory Design and Technology", John Wiley, 2004
3. Microsystem Design by Stephen D. Senturia, Springer International, Edition,2010.

Reference Books:

1. Marc Madou, ―Fundamentals of Micro Fabrication‖ CRC Press
2. Mohamed Gad-el-Hak, ―The MEMS Handbook‖, CRC Press
3. Julian W.Gardner, Vijay K.Varadan, Osama O. AwadelKarim, "Micro sensors MEMS and Smart Devices", John Wiby& sons Ltd., 2001.
4. Iannacci, J. (2013). *Practical guide to RF-MEMS*. John Wiley & Sons.

II Sem.	Design for Testability (Elective-III)	Course Code: V21ESVT12	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome:

The students will be able to

- CO1: Interpret the concepts of modelling digital circuits and simulation. **(K2)**
- CO2: Describe modelling of faults and its testing for SSF. **(K2)**
- CO3: Explain various techniques of testing. **(K2)**

UNIT-I: Modeling:

Modeling digital circuits at logic level, register level and structural level. Levels of modeling.

Logic Simulation: Types of simulation, delay models, element evaluation, hazard detection, gate level event driven simulation.

UNIT-II: Fault Modeling:

Logic fault models, fault detection and redundancy, fault equivalence and fault location. Single stuck and multiple stuck – fault models. Fault simulation applications, general techniques for combinational circuits.

UNIT-III: Testing for Single Stuck Faults (SSF):

Automated test pattern generation (ATPG/ATG) for SSFs in combinational and sequential circuits, functional testing with specific fault models. Vector simulation – ATPG vectors, formats, compaction and compression, selecting ATPG tool.

UNIT-IV: Design for Testability:

Testability trade-offs techniques. Scan architectures and testing – controllability and observability, generic boundary scan, fully integrated scan, storage cells for scan design. Board level and system level DFT approaches. Boundary scans standards. Compression techniques – different techniques, syndrome test and signature analysis.

UNIT-V: Built-in-Self-Test (BIST):

BIST concepts and test pattern generation, specific BIST architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, RTD, SST, CATS, CSTP, BILBO. Brief ideas on some advanced BIST concepts and design for self-test at board level.

Reference Books

1. MironAbramovici, Melvin A.Breur, Arthur D.Friedman, Digital Systems Testing and Testable Design, Jaico Publishing House, 2001.
2. Michael L.Bushnell, VishwaniD.Agrawal, Essentials of Electronic Testing, Springer, 2000.
3. Michael D.Ciletti, Modeling, Synthesis, and Rapid Prototyping with the Verilog HDL. Prentice Hall, 1999.

II Sem.	Semiconductor Memory Design and Testing (Elective-III)	Course Code: V21ESVT13	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome:

The students will be able to

- CO1: Describe concepts of volatile and non-volatile memory technologies. **(K2)**
- CO2: Discuss the fault modelling and testing memory devices. **(K2)**
- CO3: Explain the reliability and radiation effects of memory devices. **(K2)**
- CO4: Describe the advanced memory technologies. **(K2)**
- CO5: Describe the High-density Memory Packing Technologies **(K2)**

UNIT-I: Random Access Memory Technologies

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II: Non-volatile Memories

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

UNIT-III: Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance

RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, nonvolatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory.

UNIT-IV: Semiconductor Memory Reliability and Radiation Effects

General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and

Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation. Dosimetry, Water Level Radiation Testing and Test structures.

UNIT-V: Advanced Memory Technologies and High-density Memory Packing Technologies

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

TEXT BOOKS:

1. Semiconductor Memories Technology – Ashok K. Sharma, 2002, Wiley.
2. Advanced Semiconductor Memories – Architecture, Design and Applications - Ashok K. Sharma- 2002, Wiley.
3. Modern Semiconductor Devices for Integrated Circuits – Chenming C Hu, 1st Ed, Prentice Hall.

II Sem.	Hardware Software Co-Design (Elective-IV)	Course Code:V21ESVT14	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome:

The students will be able to

- CO1: Describe co-design architectures, methods and algorithms. **(K2)**
- CO2: Describe prototyping emulation and target architecture using embedded Systems. **(K2)**
- CO3: Explain the compilation techniques. **(K2)**
- CO4: Distinguish the various design specifications and verifications. **(K2)**
- CO5: Describe the system level specifications and design using languages. **(K2)**

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UNIT-I: Co- Design Issues:

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT-II:

Prototyping and Emulation Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure

Target Architectures Architecture Specialization techniques, System Communication infrastructure, target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60) and Mixed Systems.

UNIT-III:

Compilation Techniques and Tools for Embedded Processor Architectures Modern embedded architectures, embedded software development needs, compilation technologies and practical consideration in a compiler development environment.

UNIT-IV:

Design Specification and Verification Design, co-design, the co-design computational model, concurrency coordinating con current computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT-V:

Languages for System-Level Specification and Design-I System-level specification, design representation for system level synthesis, system level specification languages.

Languages for System-Level Specification and Design-II

Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:

1. Hardware / Software Co- Design Principles and Practice – JorgenStaunstrup, Wayne Wolf – 2009, Springer.

2. Hardware / Software Co- Design - Giovanni De Micheli, MariagiovannaSami, 2002, Kluwer Academic Publishers.

REFERENCE BOOKS:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R.Schaumont - 2010 – Springer Publications.

II Sem.	Embedded Computing (Elective-IV)	Course Code:V21ESVT15	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome:

The students will be able to

- CO1: Understand the concepts of Linux OS programming –**[K2]**
- CO2: Describe the different software development tools **[K2]**
- CO3: Explain different interfacing modules – **[K2]**
- CO4: Discuss the networking basics –**[K2]**
- CO5: Explain the basic concepts of LPC17xx Microcontroller –**[K2]**

UNIT-I

Programming on Linux Platform:

System Calls, Scheduling, Memory Allocation, Timers, Basics of Embedded Linux, Root File System, Busy Box.

UNIT-II

Introduction to Software Development Tools

GNU GCC,make, gdb, static and dynamic linking, C libraries, compiler options, code optimization switches.

UNIT-III

Interfacing Modules

Sensor and actuator interface, data transfer and control, GSM module interfacing with data processing and display.

UNIT-IV

Networking Basics

Sockets, ports, UDP, TCP/IP, client server model, socket programming.

UNIT-V

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

TEXT BOOKS:

1. Modern Embedded Computing - Peter Barry and Patrick Crowley, 1st Ed., Elsevier/Morgan Kaufmann, 2012.
2. Linux Application Development - Michael K. Johnson, Erik W. Troan, Adission Wesley, 1998.
3. Assembly Language for x86 Processors by Kip R. Irvine

REFERENCE BOOKS:

1. Operating System Concepts by Abraham Silberschatz, Peter B. Galvin and Greg Gagne.
2. Technical references and user manuals on www.arm.com.
3. The Design of the UNIX Operating System by Maurice J. Bach Prentice-Hall
4. UNIX Network Programming by W. Richard Stevens.

II Sem.	Communication Buses and Interfaces (Elective-IV)	Course Code: V21ESVT16	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcomes:

At the end of the course, students will be able to:

- CO1: Identify a particular serial bus suitable for a particular application. **(K3)**
- CO2: Develop APIs for configuration, reading and writing data onto serial bus. **(K3)**
- CO3: Design and develop peripherals that can be interfaced to desired serial bus. **(K3)**
- CO4: Describe the Different Data Transfer types and Descriptor Types **(K2)**
- CO5: Explain Data streaming Serial Communication Protocol **(K2)**

UNIT-I

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features Limitations and applications of RS232, RS485, I2C , SPI

UNIT-II: CAN

ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

UNIT-III: PCI

Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT-IV: USB

Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, isochronous transfer. Enumeration- Device detection, Default state, addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

UNIT-V

Data streaming Serial Communication Protocol- Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

TEXTBOOKS

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- JanAxelson, Lakeview Research, 2nd Ed.,

REFERENCES

1. USB Complete – Jan Axelson, Penram Publications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

II Sem.	Analog and Digital CMOS VLSI Design Lab	Course Code: V21ESVL03	L	T	P	C
			0	0	4	2

Syllabus Details

Course Outcomes: After Successful completion of the Course, the student will be able to:

- CO1 -Analyse the Characteristics of MOS Device **(K3)**
- CO2 -Analyse the basic MOS Amplifiers and current mirrors **(K3)**
- CO3 -Design the various MOS Amplifiers. **(K4)**
- CO4 -Demonstrate various CMOS combinational Digital circuits **(K2)**
- CO5- Demonstrate various CMOS Sequential Digital circuits **(K2)**

The students are required to design and implement the Circuit and Layout of any 10Experiments using CMOS 130nm Technology with Mentor Graphics Tool/Cadence/ Synopsys/Industry Equivalent Standard Software.

List of Experiments:

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
5. Simple current mirror
6. Cascade current mirror.
7. Wilson current mirror.
8. Differential Amplifier.
8. Full Adder
9. RS-Latch
10. Clock Divider
11. JK-Flip Flop
12. Synchronous Counter
13. Asynchronous Counter
14. Static RAM Cell

II Sem.	Real Time Operating Systems Lab	Course Code:V21ESVL04	L	T	P	C
			0	0	4	2

Syllabus Details

- The Students are required to write the programs using C-Language according to the Experimentrequirements using RTOS Library Functions and macros ARM-926 developer kits and ARMCortex.
- The following experiments are required to develop the algorithms, flow diagrams, source codeand perform the compilation, execution and implement the same using necessary hardware kitsfor verification. The programs developed for the implementation should be at the level of anembedded system design.
- The students are required to perform at least SIX experiments from Part-I and TWO experimentsfrom Part-II.

List of Experiments:

Part-I:

Experiments using ARM-926 with PERFECT RTOS

1. Register a new command in CLI.
2. Create a new Task.
3. Interrupt handling.
4. Allocate resource using semaphores.
5. Share resource using MUTEX.
6. Avoid deadlock using BANKER‟S algorithm.
7. Synchronize two identical threads using MONITOR.
8. Reader'sWrite's Problem for concurrent Tasks.

Part-II

Experiments on ARM-CORTEX processor using any open source RTOS. (Coo-Cox-Software-Platform)

1. Implement the interfacing of display with the ARM- CORTEX processor.
2. Interface ADC and DAC ports with the Input and Output sensitive devices.
3. Simulate the temperature DATA Logger with the SERIAL communication With PC.
4. Implement the developer board as a modem for data communication using Serial port communication between two PC‟s.

Lab Requirements:

Software:

- Eclipse IDE for C and C++ (YAGARTO Eclipse IDE), Perfect RTOS Library, COO-COX Software Platform, YAGARTO TOOLS, and TFTP SERVER.
- LINUX Environment for the compilation using Eclipse IDE & Java with latest Version.

Hardware:

- The development kits of ARM-926 Developer Kits and ARM-Cortex Boards.
- Serial Cables, Network Cables and recommended power supply for the board.

III Semester
SYLLABUS

III Sem.	IoT and its Applications	Course Code: V21ESVT17	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome: The student will be able to

- CO1: Describe M2M and IOT Technologies. **[K2]**
- CO2: Explain the layers, protocols and communication technologies in IOT. **[K2]**
- CO3: Illustrate various hardware components required for IOT applications**. [K2]**
- CO4: Discuss the cloud technologies and their services. **[K2]**
- CO5: Explain the IoT Applications. **[K2]**

UNIT-I INTRODUCTION [1, 2]
Introduction from M2M to IoT - An Architectural Overview, building architecture, Main design principles and needed capabilities, An IoT architecture outline, M2M and IoT Technology Fundamentals; Sensors, Actuators, RFID, Wireless Sensor Networks, Devices and gateways.

UNIT-II IOT PROTOCOLS & COMMUNICATION TECHNOLOGIES [2, 4]
Functionalityof Layers in IoT, IoT Connectivity – IEEE 802.15.4, Wi-Fi, Bluetooth, Zigbee, LPWAN, 5G.
Study of protocols - 6LoWPAN, CoAP, MQTT.

UNIT-III DESIGN AND DEVELOPMENT [3, 4]
Design Methodology, Embedded computing logic, IoT system building blocks, Raspberry Pi - Board details, sensor/actuator Interface using Python Programming.

UNIT-IV Cloud Computing [3, 4]
Structured Vs. Unstructured Data and Data in Motion Vs. Data in Rest, Role of Machine Learning; Data Collection, Storage and Computing Using a Cloud Platform for IoT Applications/Services, AWS for IoT – Introduction to Amazon EC2.

UNIT-V IOT APPLICATIONS [2, 3]
CASE STUDIES/INDUSTRIAL APPLICATIONS: Case Studies - Home appliances, Smart and Connected Cities, Public Safety, Agriculture, Introduction to Industry 4.0.

TEXTBOOKS:

1. Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stefan Avesand, StamatisKarnouskos, David Boyle, “From Machine-to-Machine to the Internet of Things: Introduction to a New Age of Intelligence”, 1st Edition, Academic Press, 2014.
2. IoT Fundamentals: Networking Technologies, Protocols, and Use Cases for the Internet Of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Robert Barton, Jerome Henry and Cisco Press 800 East 96th Street Indianapolis, Indiana 46240 USA
3. Daniel Minoli, “Building the Internet of Things with IPv6 and MIPv6: The Evolving World Of M2M Communications”, ISBN: 978-1-118- 47347-4, Willy Publications
4. IOT (Internet of Things) Programming: A Simple and Fast Way of Learning IOT by David Etter(Author)
5. Internet of Things - By Raj Kamal, McGraw-Hill Education. Copyright.

REFERENCE BOOKS:

1. From Internet of Things to Smart Cities: Enabling Technologies - edited by Hongjian Sun, Chao Wang, Bashar I. Ahmad, CRC Press -2018.
2. Peter Waher, “Learning Internet of Things”, PACKT publishing, BIRMINGHAM
3. Bernd Scholz-Reiter, Florian Michahelles, “Architecting the Internet of Things”, ISBN 978-3-642-19156-5 e-ISBN 978-3-642-19157-2, Springer
4. Vijay Madisetti and ArshdeepBahga, “Internet of Things (A Hands-on- Approach)”, 1st Edition, VPT, 2014.

III Sem.	Low Power VLSI Design	Course Code: V21ESVT18	L	T	P	C
			3	0	0	3

Syllabus Details

Course Outcome:

The students will be able to

- CO1: Identify various sources of power consumption **(K2)**
- CO2: Estimate the power consumption sing simulation and probabilistic Approaches**.(K2**)
- CO3: Discuss low power design at various levels of abstraction**. (K2)**
- CO4: Discuss clock distribution for low power dissipation. **(K2)**
- CO5: Describe the Algorithm &architectural level methodologies **(K2)**

UNIT-I: Introduction

Need for low power VLSI chips, Sources of power dissipation. Emerging Low power approaches. Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT-II: Power estimation Simulation Power analysis:

SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation.

Probabilistic power analysis:

Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT-III: Low Power Design Circuit level:

Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library

Logic level:

Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

UNIT-IV: Low power Architecture & Systems:

Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.

UNIT-V: Low power Clock Distribution:

Power dissipation in clock distribution, single driver vs. distributed buffers, Zero skew vs. tolerable skew, chip & package co design of clock network

Algorithm &architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

TEXTBOOKS:

1. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002
2. Rabaey, Pedram, “Low power design methodologies” Kluwer Academic, 1997

REFERENCES BOOKS:

1. Kaushik Roy, Sharat Prasad, “Low-Power CMOS VLSI Circuit Design” Wiley, 2000